Using 2D/3D technology to overcome challenges of large-area panel inspection and metrology

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The United States is seeking to breathe new life into its domestic semiconductor packaging sector with the National Advanced Packaging Manufacturing Program (NAPMP), an initiative to "establish and accelerate domestic capacity for advanced packaging substrates and substrate materials," according to a Commerce Department announcement from earlier this year [1]. In part, this program is the result of two very distinct trends, both of which are high-priority pursuits for governments and manufacturers. On the one hand, many nations like the U.S. are looking to shore up their semiconductor manufacturing capabilities to better protect themselves from potential geopolitical complications. Still another consideration is today's rapidly growing demand for high-end applications like artificial intelligence (AI) and high-performance computing (HPC) that are driving the need for advanced packages with 2.5 and 3D architectures. Such structures are built upon advanced integrated circuit substrates (AICS). Furthermore, the coming era of glass core substrates in advanced packaging will offer another level of challenges. The future is coming, and few want to be left behind.

The role of advanced packaging

Manufacturers are turning to advanced packages to help them meet the increasingly stringent requirements of today and tomorrow's 2.5D and 3D packages designed for the demanding HPC and explosive AI sectors, both of which have specifications that traditional inspection solutions struggle to meet.

With each new advanced node and accompanying shrinking transistor size, the single-chip approach grows more complicated and expensive, some might even say cost prohibitive. These applications have rigorous performance requirements, and the industry is tirelessly working to push these technologies to their full potential. Each technological advancement requires improved compute power with increased speed, lower latency, higher bandwidth and lower energy consumption. These requirements lead us to chiplets.

Chiplet-based architectures on AICS offer a cost-effective alternative to the monolithic chip by serving up a final singular packaged product with dies of different functionalities and nodes, thereby raising the overall functionality and device performance to the critical level for HPC and AI. All of this helps drive advances in panel-level packaging.

The advances noted above result in a number of challenges. The amount of AICS real estate needed to serve several dies on one substrate requires large packages, as big as 150mm x 150mm currently, with a potential to reach up to 240mm x 240mm. Additionally, each AICS may have up to 24 build-up layers, and with that comes possible complications from panel warpage, as well as the standard killer defects that plague devices. As with most things semiconductor, interconnect density is also increasing with line/space (l/s) decreasing to 5/5µm and below, pushing process control limits to the edge.

In this article, we will discuss how Onto's Firefly® G3 inspection system, a high-sensitivity automated optical inspection (AOI) panel solution containing embedded 2D and 3D metrology technologies, enables packaging houses to meet, head on, these new process control challenges posed by large, advanced packages. Included in this is the ability to better detect process excursions and fine-tune each step of the high-volume manufacturing (HVM) process to correct errors and minimize yield loss.

An AOI solution

The AOI solution discussed in this article addresses multiple inspection applications after various critical steps within the AICS process flow, including the lamination of Ajinomoto build-up film (ABF), desmearing laser drilled vias, dry-film photoresist lamination, Cu patterning and development, and Cu etching. We will also discuss the need for metrology solutions during this process.

In our investigation, we employed an optical inspection system utilizing a high-speed focus tracking system to maintain the correct distance between the imaging optics and the area being scanned. This is done to keep the image focused in real time, especially on highly-warped AICSs. The system contains multiple illumination channels to find hard-to-detect defects, some of which are not visible under traditional brightfield (BF) and darkfield (DF) illuminations.

Imaging is accomplished using a high-resolution line scan camera. The optical design provides manufacturers with technology extendibility and the flexibility to utilize the system for HVM process control, while also providing the capability to tackle R&D process optimization challenges in 2µm l/s. The multiple 3D metrology sensors provide additional data to characterize and monitor dielectric thickness, metal trace height, defect height measurement and 100% bump height metrology for the final interconnect layer. Finally, the handling flexibility of the system allows it to accommodate copper-clad laminate (CCL) and glass-core substrates, making it well-positioned for the next technology inflection in AICS technology.

Inspection, metrology and the process flow

Before we get into the particulars of this AOI system, the general manufacturing process flow for AICS, starting from the first build-up layer, is shown in **Figure 1**. The defects that can be introduced across the entire process vary based on the nature of each step. Some of the noncritical defects in earlier steps can evolve into killer defects at a later stage of the manufacturing process, resulting in a final device yield loss.

For the build-up film and dry-film photoresist lamination steps, underfilm bubbles and particles can become process pain points. After the laser drill and desmear steps, there is a need to ensure that vias are residue free. Following the patterning and development of the photoresist, residue, opens and shorts are all potential obstacles to be addressed before proceeding to the next step of Cu electrochemical plating and seed layer etching. Upon completion of the Cu plating and seed layer etching steps, Cu trace opens, shorts and seed residue add to the challenges that need to be identified, first, and then corrected. Typically, BF and DF illumination are used to identify these types of defects; however, for our purposes, we will also be exploring the use of our proprietary Clearfind® (CF) technology.

Both BF and DF techniques use light-emitting diode (LED) sources that cover the visible wavelength spectrum. In BF illumination, the image is formed by the reflected light from the sample and is a strong function of light attenuation and reflection between differing materials on the sample, while DF illumination is good at identifying small particles and defects on a flat specular surface as it scatters the light due to the oblique angle of incidence.

CF technology, however, is designed to have increased sensitivity to organic material and reduced sensitivity to interference from the surrounding nonorganic features. This creates images with high gray scale value (GSV) in organic regions and low GSV in nonorganic regions. Due to the nature of this illumination, CF has proven to be advantageous in several inspection steps during the build-up process by providing a strong signal-

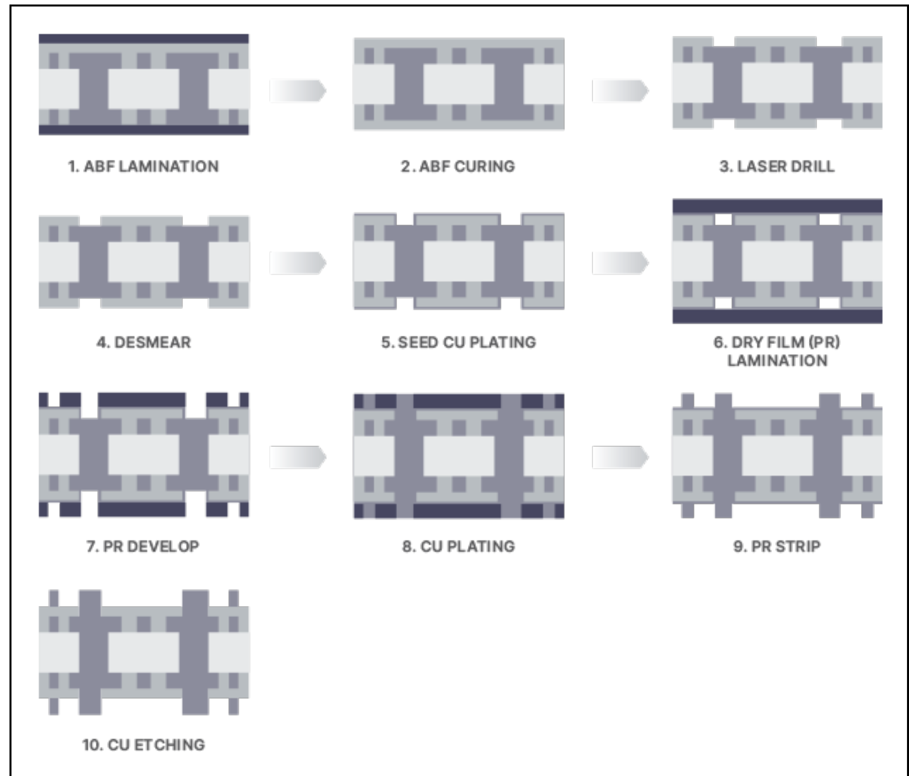

Figure 1: Typical process flow for advanced substrate build-up layers.

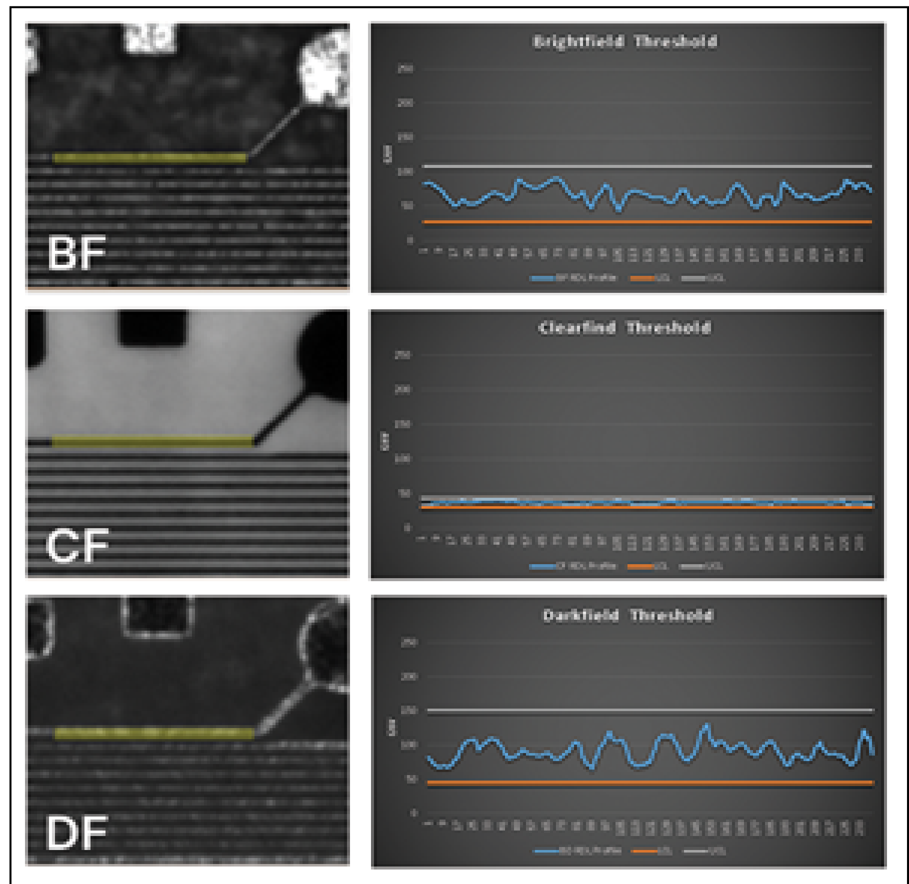

Figure 2: Noise variation on Cu trace under different illuminations.

to-noise ratio to reduce nuisance defects through the suppression of noise coming from the roughness of the Cu traces, while also detecting nonvisual organic defects (**Figure 2**).

Besides defectivity, other challenges include critical dimension variations, whether those variations involve laser-drilled vias, exposed patterns on the photoresist, or uniformity of the plated features. All of these can have a significant impact on signal integrity and the overall performance of the final device. These metrology challenges will need to be addressed during research and development and before manufacturing can begin.

ABF inspection after lamination and post desmear

ABF is a widely used insulating dielectric in AICS for flip-chip ball-grid array (FCBGA) packages. The fab environment in AICS manufacturing is not as clean as environments found in front-end fabs, so substrates are exposed to foreign particles as they move from one processing tool to another. The foreign particles can potentially be embedded underneath the ABF during the lamination process, leading to the creation of defects such as shorts and opens later in the build-up process. If the embedded particle is large enough, it can lead to a layer-to-layer short that will go unnoticed until the final electrical test (E-test). Unfortunately, at this point, it is too late to perform any rework as the substrate has gone through multiple processing steps.

While detecting embedded particles is critical, foreign particles on top of the film are considered to be nuisances because the protective film on top of the ABF is eventually removed. The challenge at this inspection step is to not only find the embedded particles, but also filter out nuisance defects from the top of the ABF so that operators don't spend valuable time reviewing and classifying noncritical defects.

A mixture of DF- and CF-based imaging has proven to be beneficial in the detection of embedded defects. The combination of the two illumination channels makes the ABF translucent, thereby enabling the system to capture defects at the bottom of the film (**Figure 3a**). Because DF scatters light off particles, the system can also easily distinguish between particles on the top of the film versus the bottom, and can be classified into rough bins using on-tool binning (**Figure 3b**). Additional image-based classification techniques are deployed using proprietary automated defect classification (ADC) software, which utilizes machine learning to identify and classify defects into finer bins. The increasing demand to lower the amount of rework and ensure high yields on AICS has led to the implementation of inline inspection at the post-lamination step.

The need to inspect vias for residual ABF is also of concern. After lamination and curing of the ABF, vias are formed by high-energy CO_2 or ultraviolet (UV) lasers to make electrical connections between layers. Occasionally, ABF is not completely removed from the via or residues remain after a non-optimal desmearing process, which results in a poor electrical connection through the via after it is filled with Cu. This, in turn, negatively affects signal integrity. Therefore, inspecting the via after laser ablation and desmear is necessary to find such defects. Residue is detectable using either CF or BF technology; however, CF is better able to detect residual ABF inside the vias. In BF illumination, organic residue becomes less prominent because of the rough Cu present at the via bottom (**Figure 4**).

After-development and after-etch inspection

As you know, dry-film resist plays a key role in the build-up process of each layer in an AICS substrate. During this process, the dry-film resist is laminated, patterned and developed on a Cu seed layer; any process excursions during patterning and development will lead to poor circuit formation in the plating step (**Figure 5**). As mentioned previously, finding all defects will require the presence of multiple illumination channels as organic residues are easily visible in CF, but other defects such as

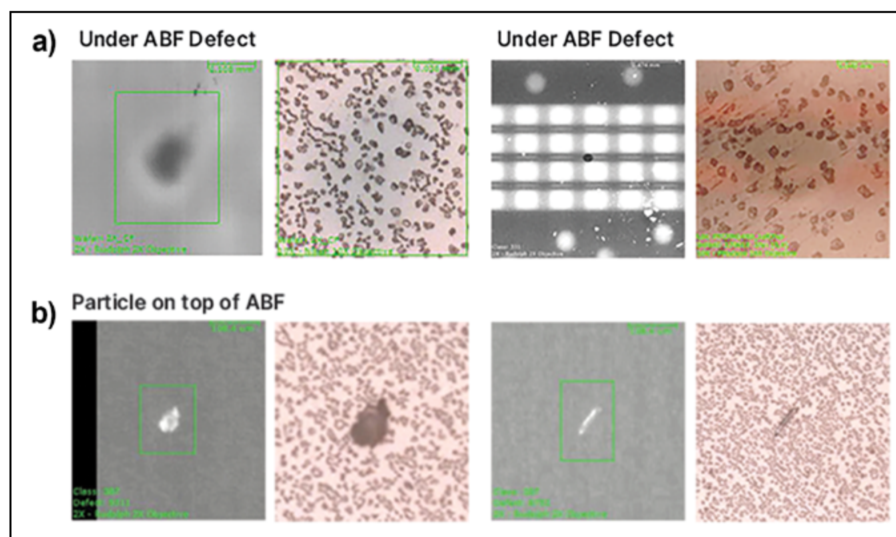

Figure 3: Examples of a) embedded defects, and b) on-surface particles.

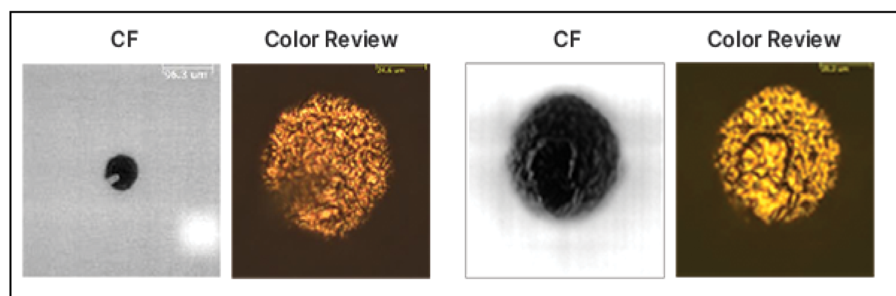

Figure 4: Examples of organic residue after desmear.

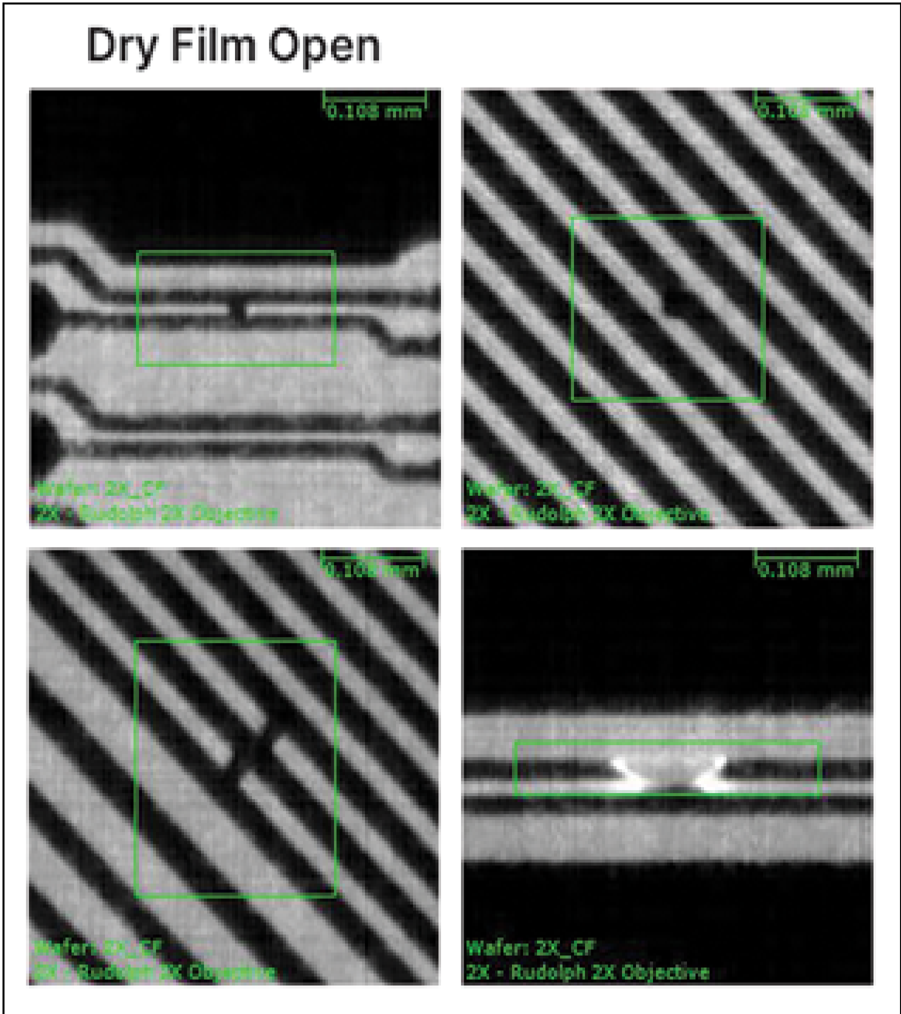

Figure 5: Examples of dry-film defects.

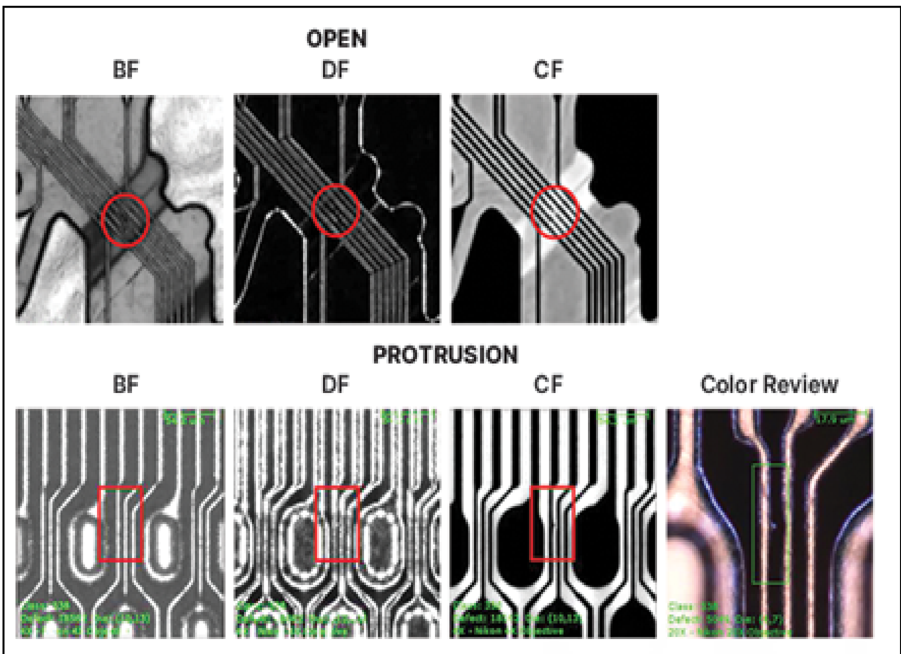

Figure 6: Examples of opens and protrusions.

scratches or damage to dry film might require BF- or DF-based technology.

With the development of the dry-film resist out of the way, the substrate enters the plating step where the Cu trace lines are formed. Afterward, the dry-film resist is removed, leaving all Cu trace lines connected by a thin Cu seed layer. This Cu seed layer needs to be etched away to complete circuits. It is very critical to accurately control the copper seed etching process to achieve fine Cu traces. Under-etching may cause shorts, while over-etching may cause large reductions in the Cu trace line or result in an open circuit. All of these defects impact device reliability. When the residual Cu extends to 30% or more into the space between Cu trace lines, this is considered a critical defect. Traditionally, BF-based inspection methodologies have been used at this inspection step, but the downside is that it results in a large number of defects, and these are often false or noncritical. This is because the surface of Cu trace lines tends to become rough and grainy after the etching process, thereby, making any variations in the brightness of the Cu line significant. In addition, dark regions in the Cu lines can be easily mistaken for open circuits.

Defect escape is also a big concern because of poor contrast and noise from the presence of multiple underlayers, which often shift due to process variation. These challenges increase exponentially as Cu lines shrink to 2µm. Because CF technology is not sensitive to the rough or grainy surface of metal, it offers a more robust inspection technology compared to BF and DF following the after-etch step to detect defects like opens, shorts, nicks and protrusions (**Figure 6**). Combining inspection with the closely-integrated ADC software allows high-sensitivity inspection to detect and classify critical defects without the hassle of performing a manual review on a large number of defects.

Another key defect of interest, and one that is also a function of an inconsistent etching process, is leftover thin Cu seed residue. The presence of thin Cu residue becomes more prevalent as the Cu trace pitch decreases. The reason for this stems from the etching process itself. This process requires a fine-tuned etching

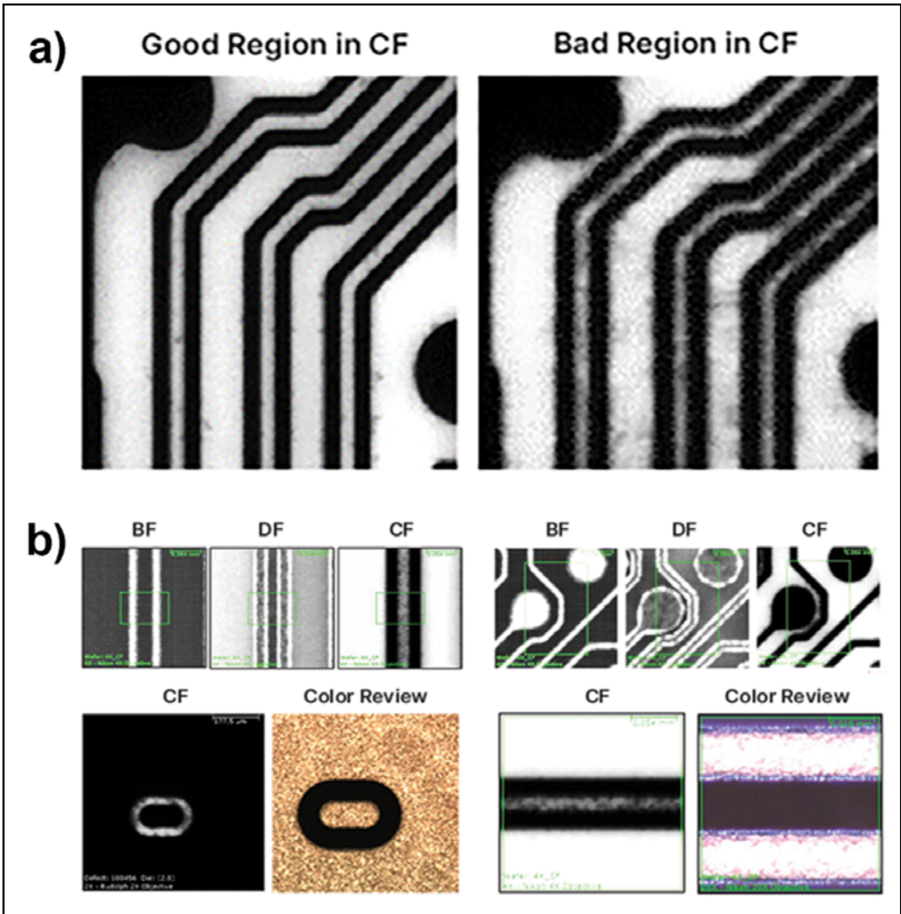

Figure 7: a) Presence of thin Cu residue; and b) Thin Cu seed residue imaged in multiple illuminations.

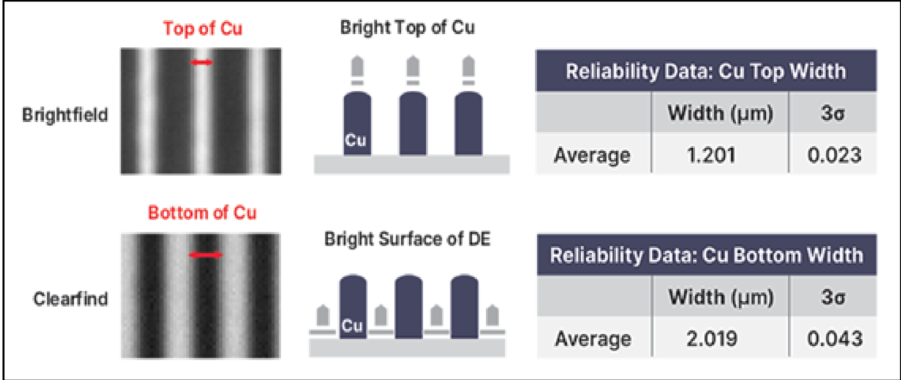

Figure 8: Critical dimension measurements for top and bottom width of Cu line.

process and chemistry to ensure that the seed metal is completely removed between the plated Cu features, which contain a combination of larger and smaller design rules. Thin Cu residue appears as a cluster of fine specular Cu particles in the region at the bottom of the Cu trace and on top of the ABF (**Figure 7a**). If there is significant accumulation of metallic residue, a device may short.

Thin Cu seed residue is not visible in traditional BF- and DF-based illuminations (**Figure 7b**). Instead, identifying this residue requires UV-based technology. This defect is often not detectable using AOI and is typically identified using a separate review station. ABF has a high GSV when excited by CF illumination; this mimics the appearance of UV-based imaging, making the thin Cu specular residue on top of the organic film easily detectable because the metallic residue exhibits low GSV. The considerable contrast in the organic space region allows high-sensitivity sub-micron inspection to detect these small metallic particles during the after-etch inspection step.

Metrology and the build-up process

The implementation of 2D- and 3D-based metrology during the build-up process is as important as defect inspection. Such techniques are needed to ensure the process is stable during research and development and before manufacturing moves to small-volume manufacturing (SVM). Metrology is also utilized to monitor degradation as the process becomes mature in HVM. Using metrology during R&D provides additional insight into the manufacturing process at various steps. Understanding the deviations, their cause, and finding solutions with the data will enable a more suitable transition to production.

Critical dimensions are used to monitor etch quality, as well as detect lens distortion in the lithography process. The AOI system employs high-resolution objectives to monitor 2µm l/s width across several points on the panel. These critical dimensions of the Cu metal line are measured for width at both the top and bottom using different illumination channels to ensure they are within specification tolerance (**Figure 8**).

Multiple types of technology exist within the 3D metrology space that are suitable in this scenario. The AOI in this discussion contains two metrology sensors that are of use: a white light interferometry sensor and a laser triangulation sensor, with each employing a different theory of operation and each targeting different applications. The system's white light interferometry sensor is used to monitor the thickness of the ABF as well as the height of the Cu metal line (**Figures 9** and **10**). The height of the metal line indicates the performance of the plating and etching process because inconsistent height can lead to signal integrity issues within the device. Meanwhile, the laser triangulation sensor enables 100% metrology for bumps/pads on the panel and is capable of determining good coplanarity before the die attach process so proper electrical connections can be formed between the chip and the AICS (**Figure 11**).

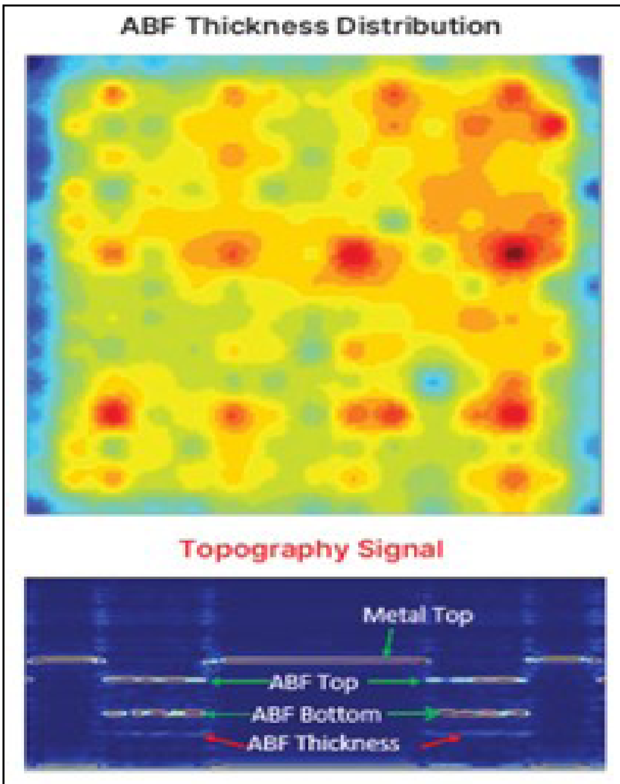

Figure 9: ABF thickness measurements.

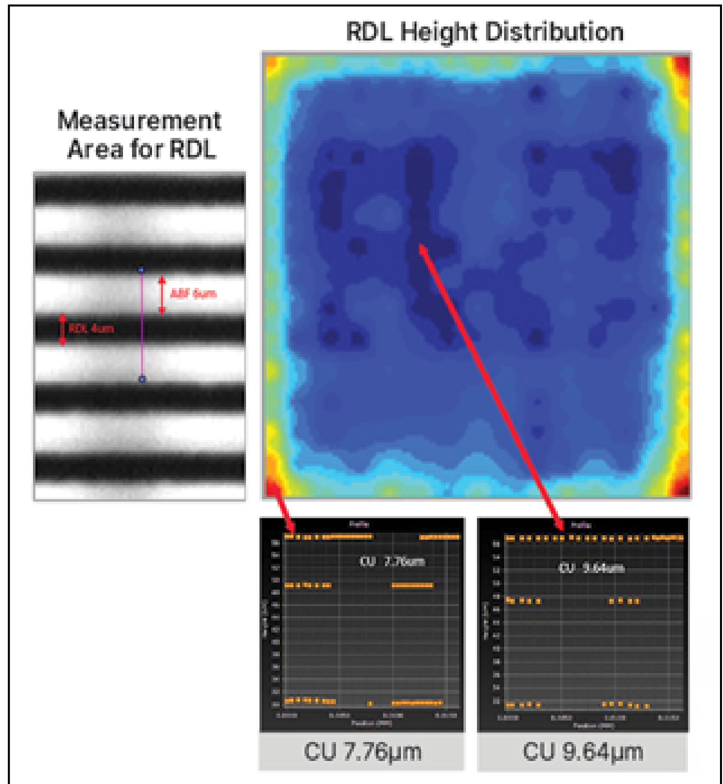

Figure 10: Cu trace height measurement.

Summary

Any nation hoping to create or revitalize domestic semiconductor production from the front end to the back end will need to devote time and resources to ensuring it has a considerable advanced packaging sector capable of meeting the needs of today and tomorrow's 2.5 and 3D packages. To accomplish such objectives, these nations will greatly benefit from the new and emerging technologies discussed in this article as they seek ways to optimize the build-up process in advanced IC substrate manufacturing.

Reference

1. "National Advanced Packaging Manufacturing Program," 28 Feb. 2024, National Advanced Packaging Manufacturing Program | NIST.

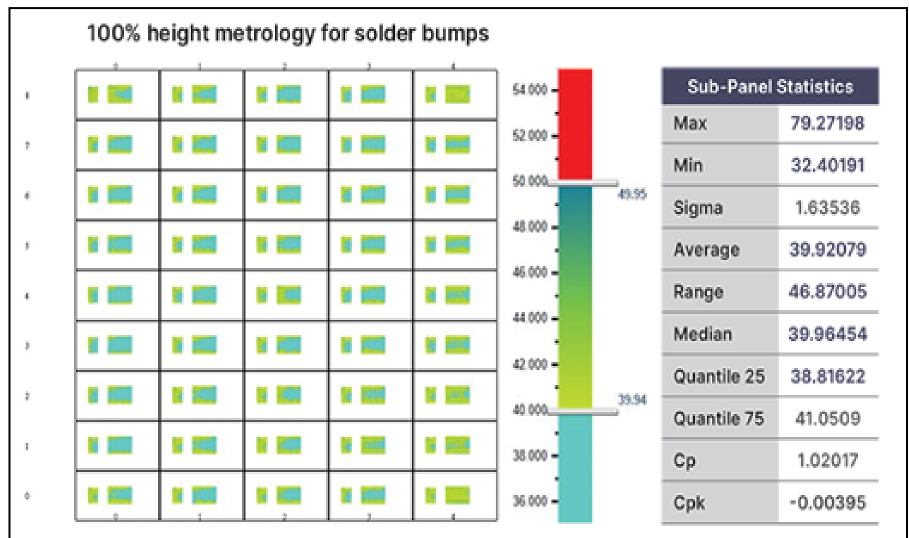

Figure 11: One hundred percent height metrology for solder bumps.

Biographies

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