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JUNE 2018

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

Optimized Stepping for Fan-out Wafer and Panel Packaging P.10

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Extension MEDIA

Optimized stepping for fan-out wafer and panel packaging

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Optimized stepping, based on parallel analysis of die placement errors and prediction of overlay errors, can increase lithography throughput by more than an order of magnitude and deliver commensurate reductions in cost of ownership. The productivity benefits of optimized stepping are demonstrated using a test reticle with known die placement errors.

Fan out wafer and panel level packaging (FOWLP/FOPLP) processes place individual known good die on reconstituted wafer (round) or panel (rectangular) substrates, providing more space between die than the original wafer. The additional space is used to expand (fan out) the die's I/O connections in order to create a pad array large enough to accommodate solder balls that will connect the die to the end-use substrate. The processes used to create these redistribution layers (RDL) are similar to wafer fabrication processes, using patterns defined by photolithography, with feature sizes typically ranging from a few micrometers to tens of micrometers. The placement and reconstitution molding processes introduce significant die placement errors that must be corrected in the photolithography process to ensure accurate overlay registration among the multiple vias and distribution layers that are built up to form the RDL. The errors can be measured on the lithography tool, but this significantly impacts throughput as the measurement process for each die may take as much or more time than the exposure itself.

Current best-practice methods employ an external metrology system to measure the displacement of each die. This metrology data is converted into a stepper correction file that is sent to the lithography stepper tool, eliminating the need to measure displacement on the stepper and more than doubling stepper throughput. An important enhancement to this method, optimized stepping, varies the number of die per exposure based on a predictive yield analysis of the displacement measurements, potentially multiplying throughput 20X or more. Results obtained using a test reticle that includes intentionally displaced die pads, vias, and RDL features typical of an FOWLP/FOPLP process confirm the validity of the approach.

Introduction

Die placements on reconstituted wafer or panel substrates include translational and rotational placement errors. The pick and place process itself introduces initial error. Additional error is created in the mold process and by instability of the mold compound through repeated processing cycles. As a result, the position of the die must be measured before each exposure in the lithography system to ensure sufficient registration with the underlying layer.

Displacement errors can be measured in the lithography tool, but the measurements are slow, typically taking as much time as the exposure. Moving the measurement to a separate system and feeding corrections to the stepper can double throughput.

Optimized stepping adds predictive yield analysis to the external measurement and correction procedures and increases the number of die included in the exposure field up to a user-specified yield threshold. **FIGURE 1** illustrates the exposure/measurement loop. The measurement and analysis are repeated after each layer is exposed, calculating a new set of corrections. In addition to corrections, the software engine analyzes the displacement errors to predict yield (based on a user designated limit for acceptable registration error) for multiple die exposure fields of varying sizes. The method requires tight integration of the stepper and measurement system with the controlling software.

With RDL features currently reaching sizes as small as 2μm, die placement measurements and pattern overlay registration requirements are also continuing to tighten. The speed of the measurement/correction/prediction calculation for each wafer/panel is also an important

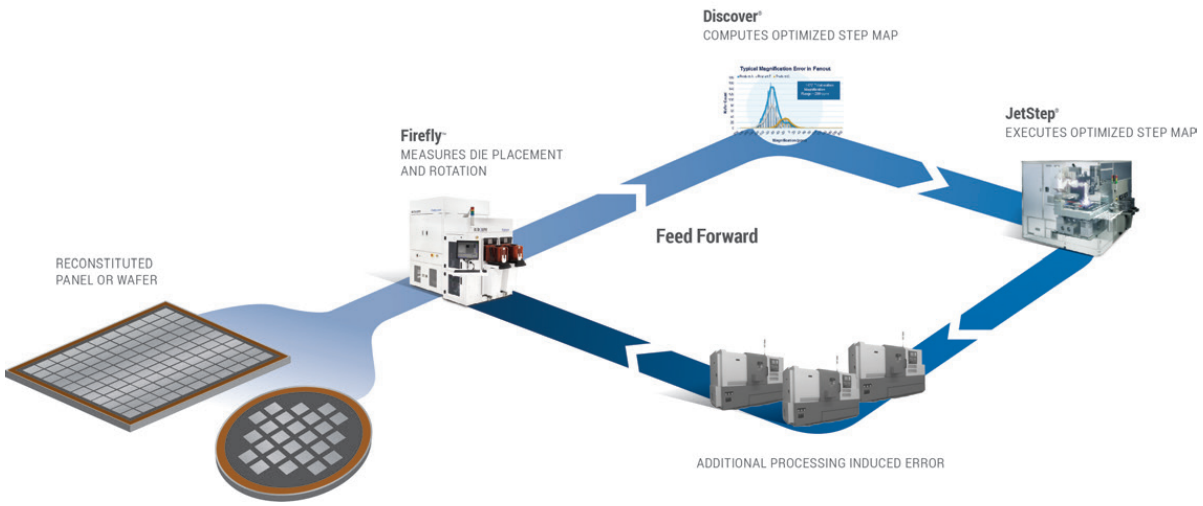

FIGURE 1. The optimized stepping process loop includes: 1) measurement of die displacement errors outside the stepper, 2) correction calculations and yield modeling, 3) exposure, 4) continuous run-to-run adjustments.

consideration. It must be faster than the exposure time to avoid becoming the throughput limiting step. Note that this requirement refers to the total exposure for multiple die per field which can be much less than the time needed to expose each die individually. The metrology system used in this work (Firefly system, Rudolph Technologies) can meet these challenges and measure placement errors for >5,000 die on a 510mm x 515mm panel in less than 10 minutes.

The stepper must be able to accept externally generated corrections for translation, rotation, and magnification. It must also have a large exposure field and the ability to automatically select different images from the reticle (masking blades), changing the size of the field for each exposure. The stepper used in this work was the JetStep system from Rudolph Technologies.

The third critical piece of the optimized stepping loop is the software engine (Discover software, Rudolph Technologies) which calculates displacement corrections and predicts yield for various multi-die exposure configurations. It also enables statistical process control (SPC) and controls genealogy.

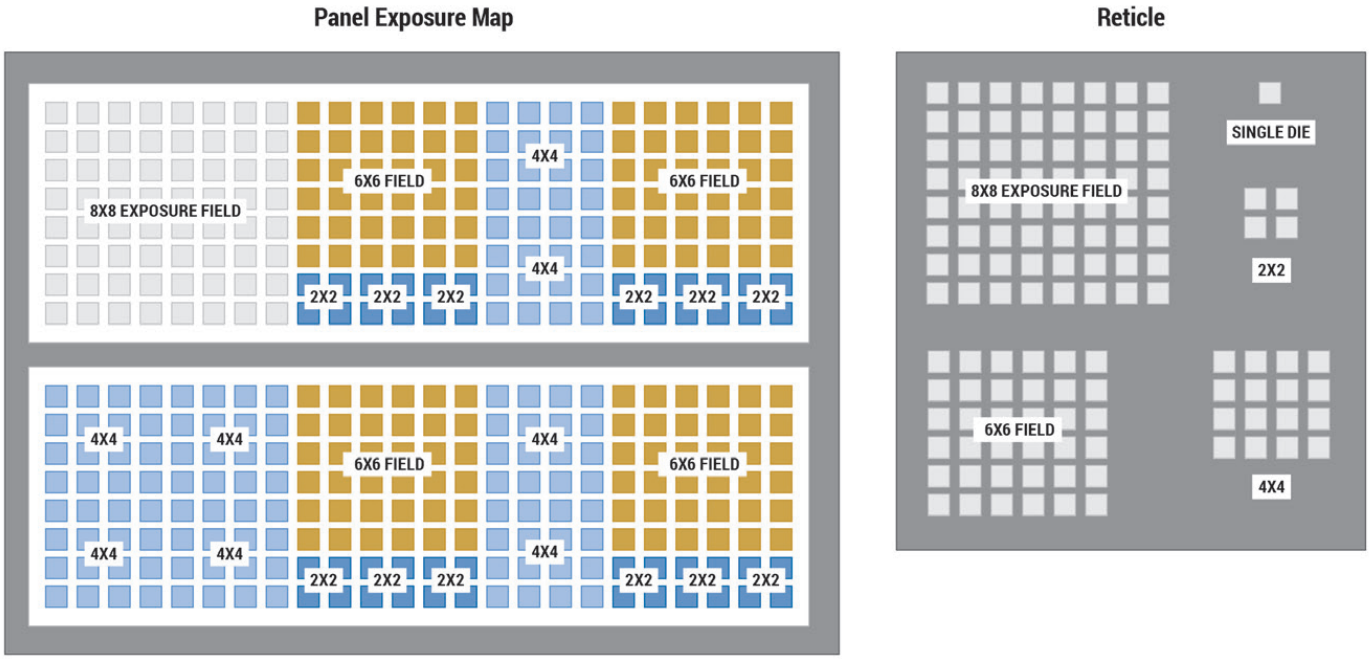

FIGURE 2. Optimized stepping uses a reticle (right) that contains multiple field sizes, each including a multi-die array of varying size (here ranging from 1X1 to 8X8). Under software control, the stepper exposes fields as required to cover the panel (left) while balancing throughput (field size) and yield (overlay error).

Exposure Shot Pyramid Example

LEVEL	MARK TYPE	PACKAGE #	FAILURE ALLOWED
1	1x1	1	0
2	1x2	2	0
3	2x2	4	0
4	4x4	16	1
5	8x8	64	4

Recursive Split Illustration

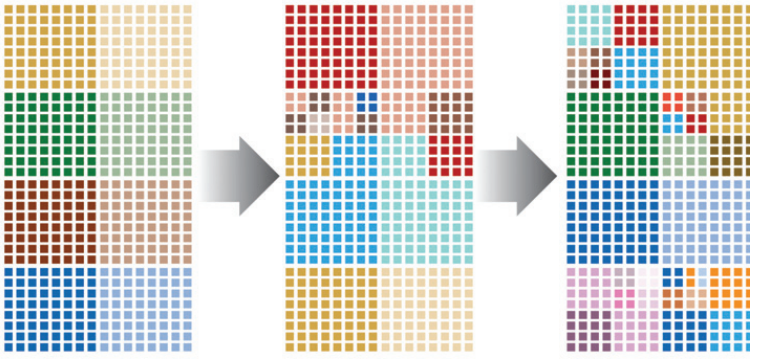

FIGURE 3. The operator specifies yield requirements in a shot pyramid that designates the maximum number of failures allowed for each field size, the software initially predicts yields at the largest field size and recursively splits the field to a smaller size if the prediction does not meet the yield requirement.

Balancing yield and throughput

Optimized stepping uses a reticle that includes multiple exposure fields each comprising die arrays of different sizes. In **FIGURE 2** the arrays range from a single die to an 8 X 8 array of 64 die. On a wafer containing random displacement errors, the smallest overlay error will be achieved by aligning the exposure pattern for each die individually. However, this accuracy comes at a high cost of reduced throughput. Optimized stepping analyzes the measured displacement errors and calculates the number of die that will meet a designated overlay error limit for various field sizes. It then selects the combination of fields that maximizes throughput. In operation, the stepper automatically selects the correct reticle image and adjusts the field size to expose the selected array.

The yield prediction algorithm (**FIGURE 3**) uses a recursive splitting procedure that initially predicts yield for the largest available field. If the prediction does not meet user-defined yield requirements, it splits the field and re-evaluates the prediction, repeating this cycle for decreasing field sizes until all exposures yield satisfactory results. The user designates an aggressiveness factor (larger values mean more aggressive splits) and specifies yield requirements in an exposure shot pyramid that determines the number of failures allowed for each available field size.

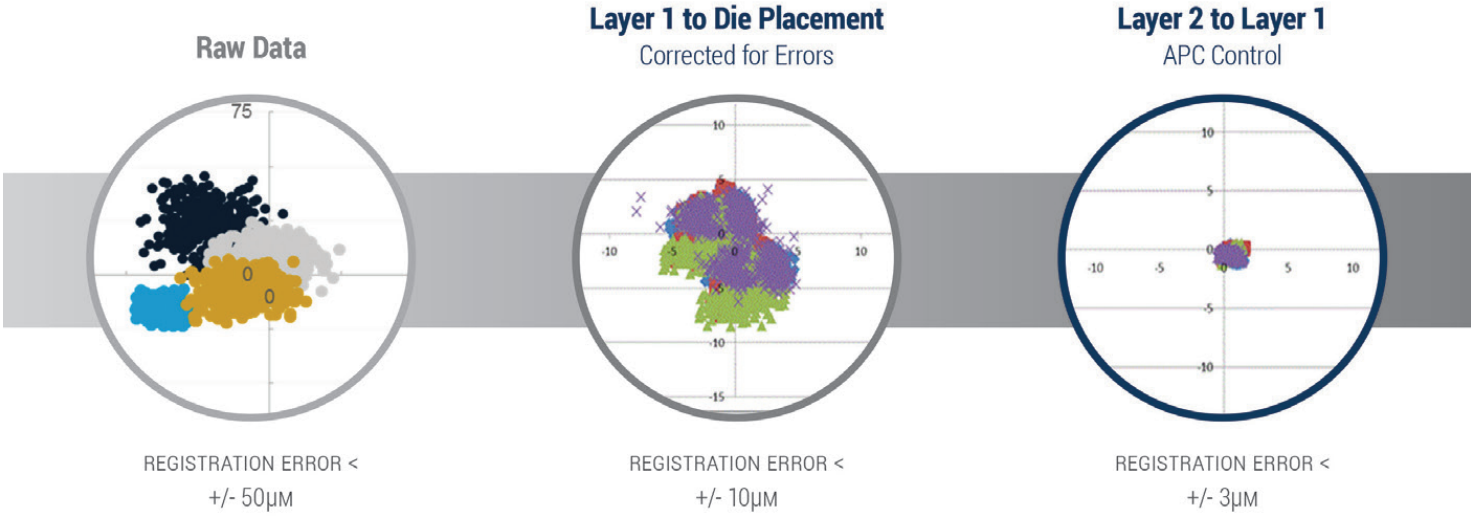

FIGURE 4. Compares registration errors for uncorrected, raw data (left), corrected exposures (middle), and APC run-to-run control (right) showing an improvement from +/-50µm to less than +/-3µm.

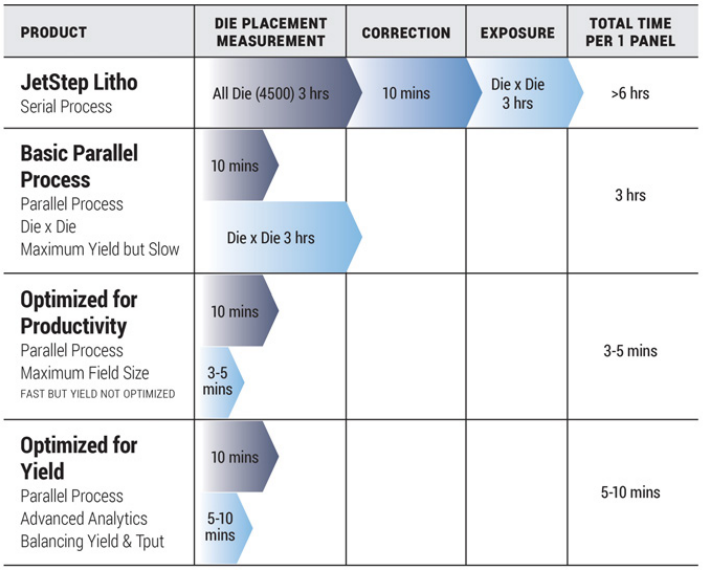

FIGURE 5. Making measurements in parallel outside the stepper cuts total cycle time in half, from six hours to three hours, and makes exposure time the rate limiting step. Optimized stepping can cut exposure time by an order of magnitude and permits the operator to balance productivity against yield.

Results

Optimized stepping was evaluated using a test reticle with multiple field sizes containing die that included pads, vias and RDL structures typical of FOWLP/FOPLP. The patterns included predefined offsets in some of the structures for feed forward measurement testing. Application of the corrections calculated from the die placement error measurements yielded overlay errors of < +/-3µm (**FIGURE 4**).

Productivity vs. yield

FIGURE 5 illustrates the potential benefits of optimized stepping applied to a panel process. In the example the panel contains approximately 4,500 die. A conventional serial process, with placement errors measured on the stepper, takes a little over six hours, including three hours for measurement and three hours for exposure. Making the measurements outside the stepper in parallel with the exposure halves the cycle time per panel to three hours, and the exposure time becomes the throughput limiting step. The third case is optimized for productivity, using larger field sizes and more relaxed yield requirements. It reduces cycle time to less than 10 minutes. The final case balances throughput against more stringent yield requirements and results slightly higher cycle times that are still nearly an order of magnitude shorter than the conventional serial process of the first case.

Conclusion

Optimized stepping can increase lithography throughput by more than an order of magnitude and deliver commensurate reductions in cost of ownership. The method also provides a means to balance productivity (throughput) against yield, adding an extra dimension of flexibility for optimizing profitability. Optimized stepping requires a stepper that can use externally calculated corrections and automatically change field size and reticle position. The metrology system must have sufficient accuracy and speed (faster than the accelerated exposure time). The control software must be able to predict yields based on measured displacement errors and control the stepper. Using a test reticle with known displacement errors, we have verified the accuracy of the metrology system and correction procedures and demonstrated the productivity benefits of optimized stepping.

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