Non-Destructive Measurement of Bottom Width in Deep Trench Isolation Structures using IRCD Metrology

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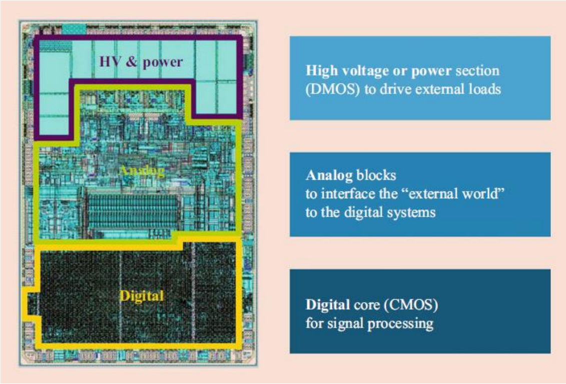
Outline

- Background
- Motivation & Problem Statement
- IRCD Metrology Technology
- Simulation Study Results
  - Conventional UV-VIS-NIR OCD vs IRCD
- Experimental Results
- Conclusion

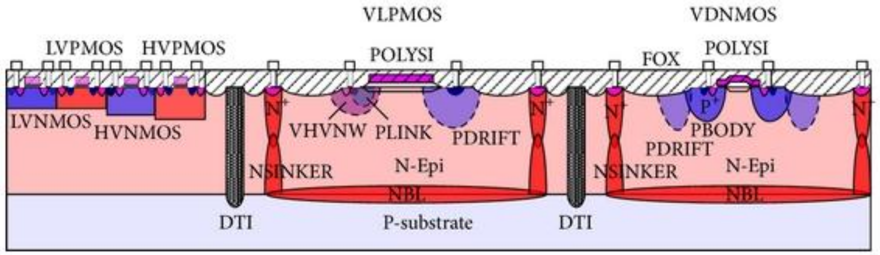
Background

What is a BCD Device? Why is DTI important?

- BCD: Bipolar, CMOS, DMOS transistors on a single chip for Smart Power IC's
  - Bipolar: Analog functionality
  - CMOS: Digital
  - DMOS: Power

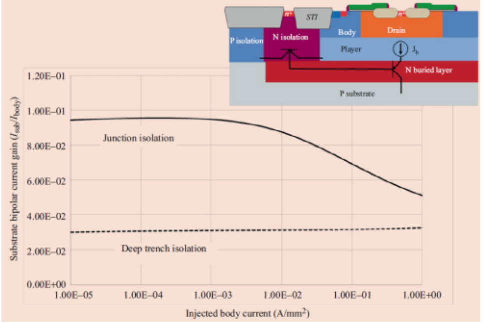


Croce, G., Andreini, A., Galbiati, P., Diazzi, C. (2023). BCD Process Technologies. In: Rudan, M., Brunetti, R., Reggiani, S. (eds) Springer Handbook of Semiconductor Devices



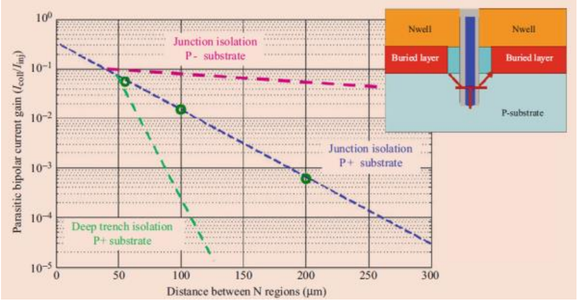
- Electrical Isolation
  - Key enabler & determines final product performance
  - DTI (Deep Trench Isolation) introduced at 0.18µm node
    - Key Benefits vs Junction Isolation:
      - Improved latch-up by:
        - Reduced substrate parasitics (Parasitic PNP bipolar gain)
        - Reduced lateral NPN bipolar gain (electron diffusion length)
      - Area density gain by reduced lateral isolation dimensions

Parasitic PNP Bipolar Gain



Croce, G., Andreini, A., Galbiati, P., Diazzi, C. (2023). BCD Process Technologies. In: Rudan, M., Brunetti, R., Reggiani, S. (eds) Springer Handbook of Semiconductor Devices

Lateral NPN Bipolar Gain



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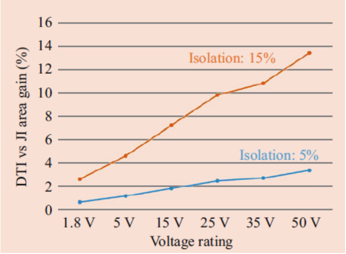
Area gain vs Voltage Rating



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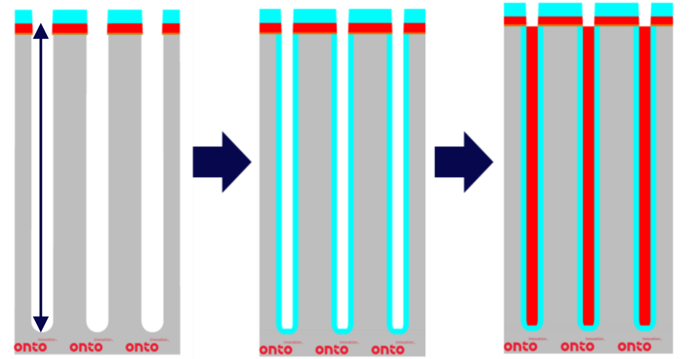
“Typical” DTI Process, Process Control & Major Issue

- Typical DTI Process
  - DRIE Etch
  - Oxide Liner Growth or Deposition
  - Poly-Silicon Deposition & Etch back

DTI Substrate Contact Process Flow



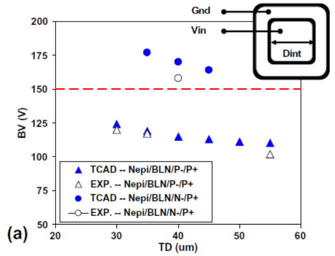
Post DTI Trench Etch

Post DTI Trench Oxide Growth

Post DTI Trench Poly-Si Fill & Etch back

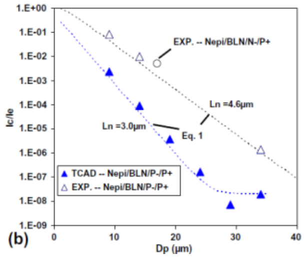
- Key Inline Metrology: DTI Depth
  - Why?
    - Depth controls Breakdown Voltage & I_c/I_e
      - Tradeoff between those parameters

BV vs DTI Depth



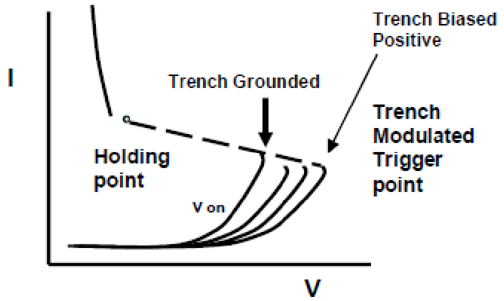
Charavel, R. *et al.* Next generation of Deep Trench Isolation for Smart Power technologies with 120 V high-voltage devices. *Microelectronics Reliability* **50**, 1758–1762 (2010).

I_c/I_e vs DTI Depth



Charavel, R. *et al.* Next generation of Deep Trench Isolation for Smart Power technologies with 120 V high-voltage devices. *Microelectronics Reliability* **50**, 1758–1762 (2010).

- Issues with the “typical” DTI process
  - Floating Gate Effect caused by capacitive coupling of poly-Si filled DTI to P/N Wells and substrate
  - Modulates trigger voltage

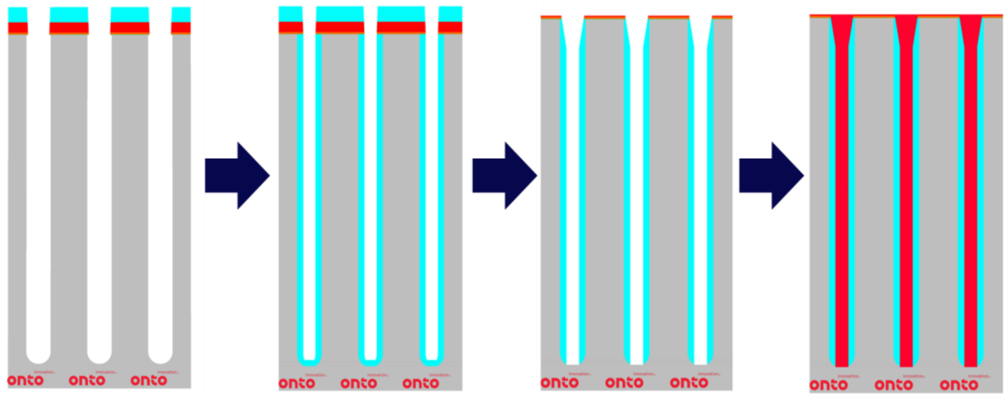


Voldman, S. H. The Influence of a Novel Contacted Polysilicon-Filled Deep Trench (DT) Biased Structure and Its Voltage Bias State on CMOS Latchup. in *2006 IEEE International Reliability Physics Symposium Proceedings* 151–158 (2006). doi:10.1109/RELPHY.2006.251208.

DTI Process Flow with Substrate Contact & Process Control

- Process Flow (Self-Aligned)
  - DRIE Etch
  - Oxide Liner Growth or Deposition
  - Contact Etch
  - Conductor Fill and Etch Back

DTI Substrate Contact Process Flow



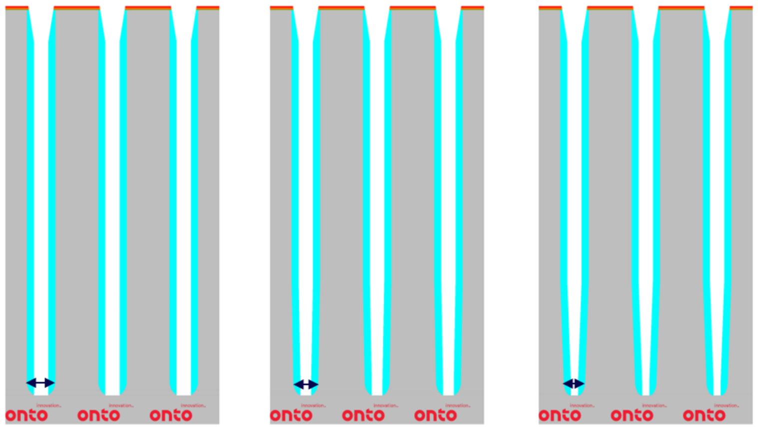
Post DTI Trench Etch

Post DTI Trench Oxide Growth

Post DTI Trench Contact Etch

Post DTI Trench Conductor Fill

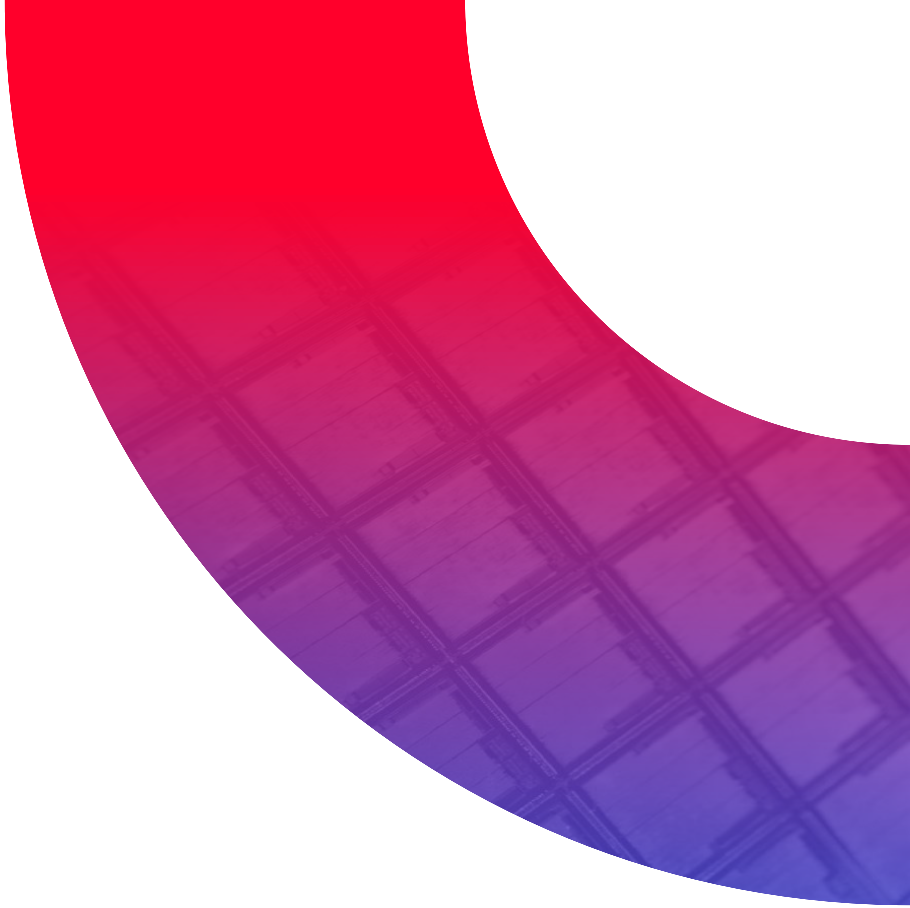
- Key Inline Metrology: DTI BCD (Post Trench Etch)
  - Why?
    - Contact resistance impacts device performance (RC delay, ect.)
    - Contact resistance is proportional to cross-sectional area
    - Smallest Trench CD will be the BCD (for this process; not the case for SOI)



Contact Etch Trench BCD POR

Contact Etch Trench BCD -

Contact Etch Trench BCD --



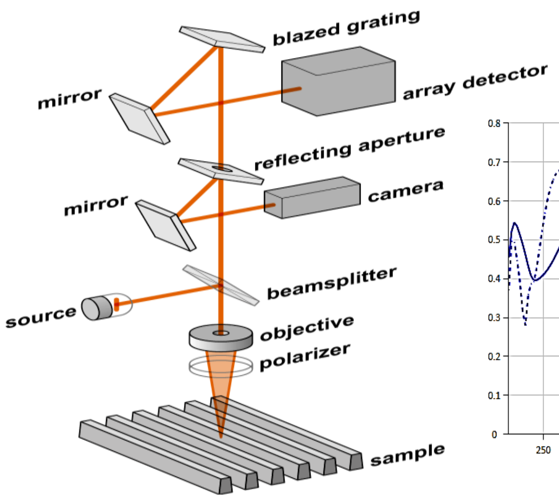
Metrology Overview

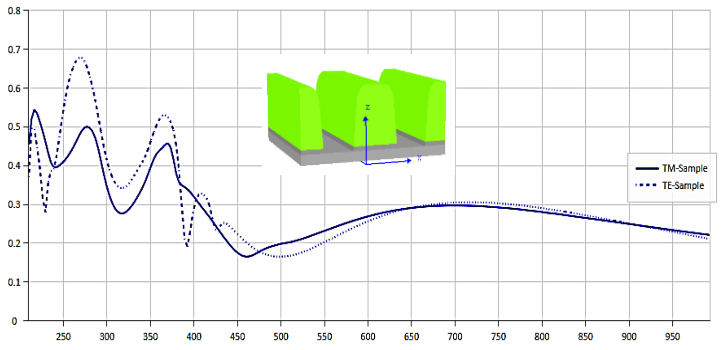
“Conventional” OCD Technology

UV-VIS-NIR Wavelength Range

Spectroscopic Reflectometry

Δ(intensity)





TE or s-polarization (normal to plane of incidence)
TM or p-polarization (parallel to plane of incidence)

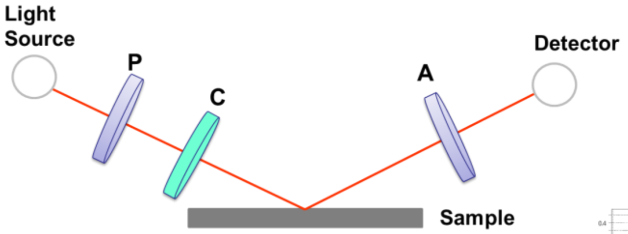
Schematic

Spectra

Spectroscopic Ellipsometry

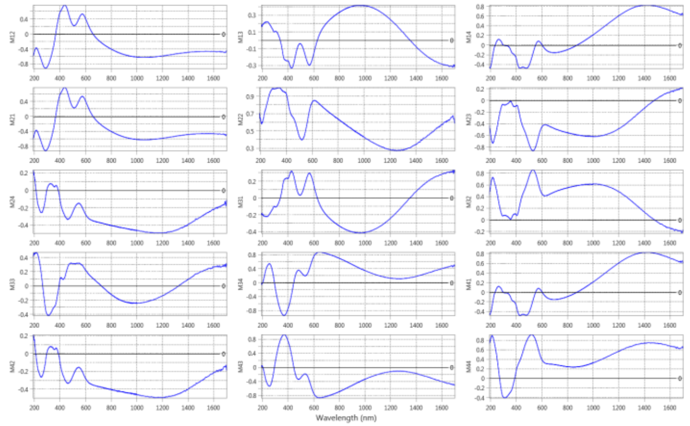
Δ(polarization state)

$$I_{out} = \frac{1}{2}[1 \quad \cos(2\theta) \quad \sin(2\theta) \quad 0] \cdot \begin{bmatrix} M11 & M12 & M13 & M14 \\ M21 & M22 & M23 & M24 \\ M31 & M32 & M33 & M34 \\ M41 & M42 & M43 & M44 \end{bmatrix} \cdot \begin{bmatrix} 1 \\ \cos(2\theta) \\ -\sin(2\theta) \\ 0 \end{bmatrix} \cdot I_o$$



Mueller Matrix

$$MM = \begin{bmatrix} M_{11} & M_{12} & M_{13} & M_{14} \\ M_{21} & M_{22} & M_{23} & M_{24} \\ M_{31} & M_{32} & M_{33} & M_{34} \\ M_{41} & M_{42} & M_{43} & M_{44} \end{bmatrix}$$



Schematic

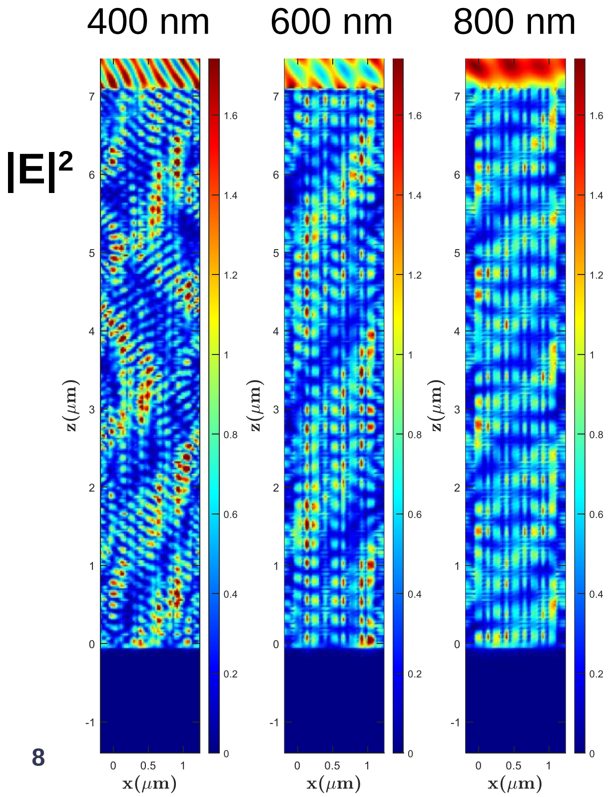
Spectra

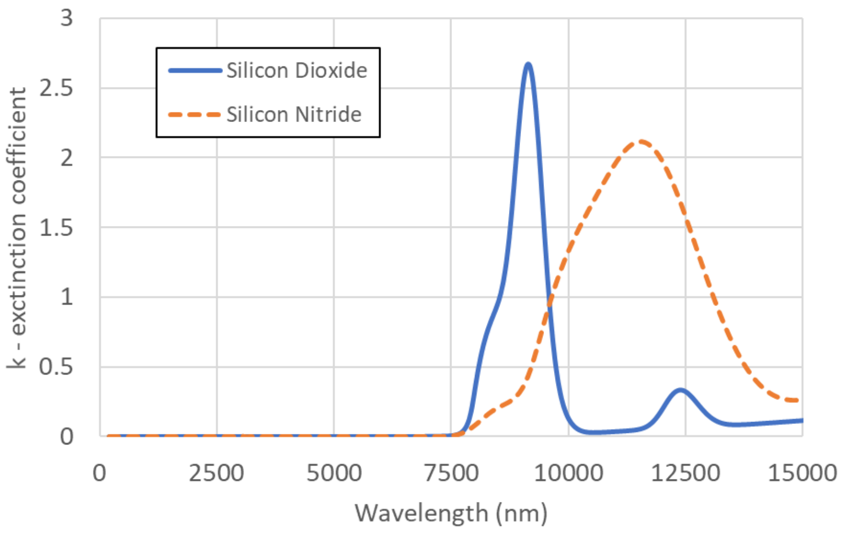
IRCD Metrology Overview

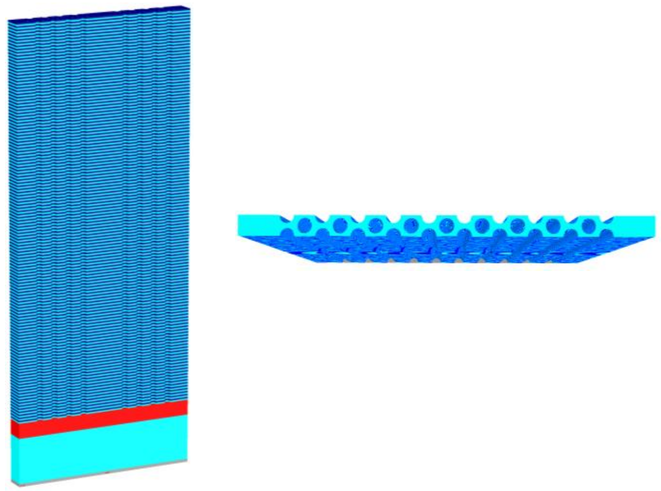
Channel Hole Etch Structure FDTD Simulation of Electric Field Intensity

Wavelengths in **OCD** range interact similarly leading to **high parameter correlation** limiting profile sensitivity

OCD



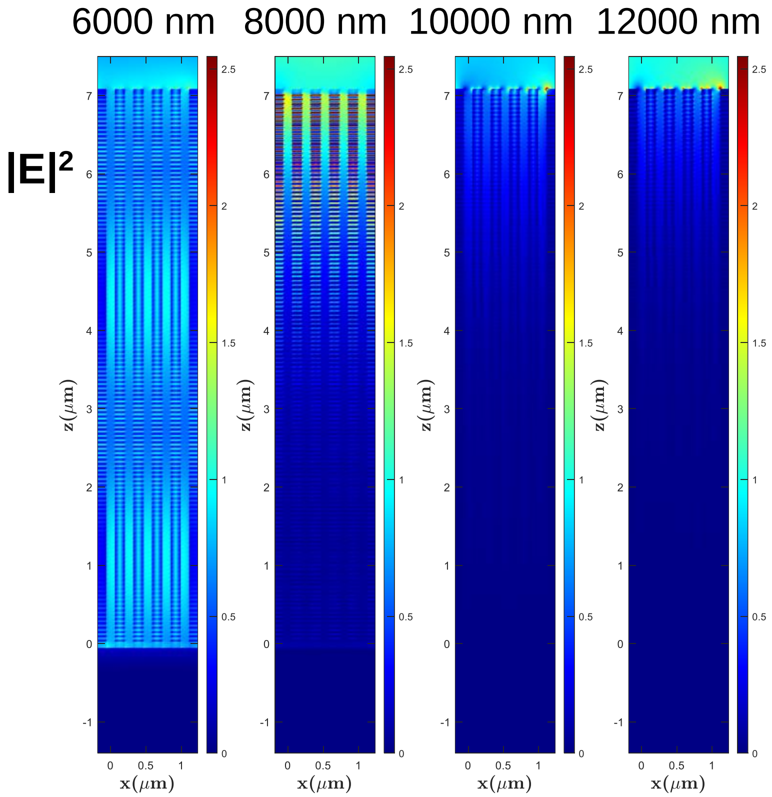


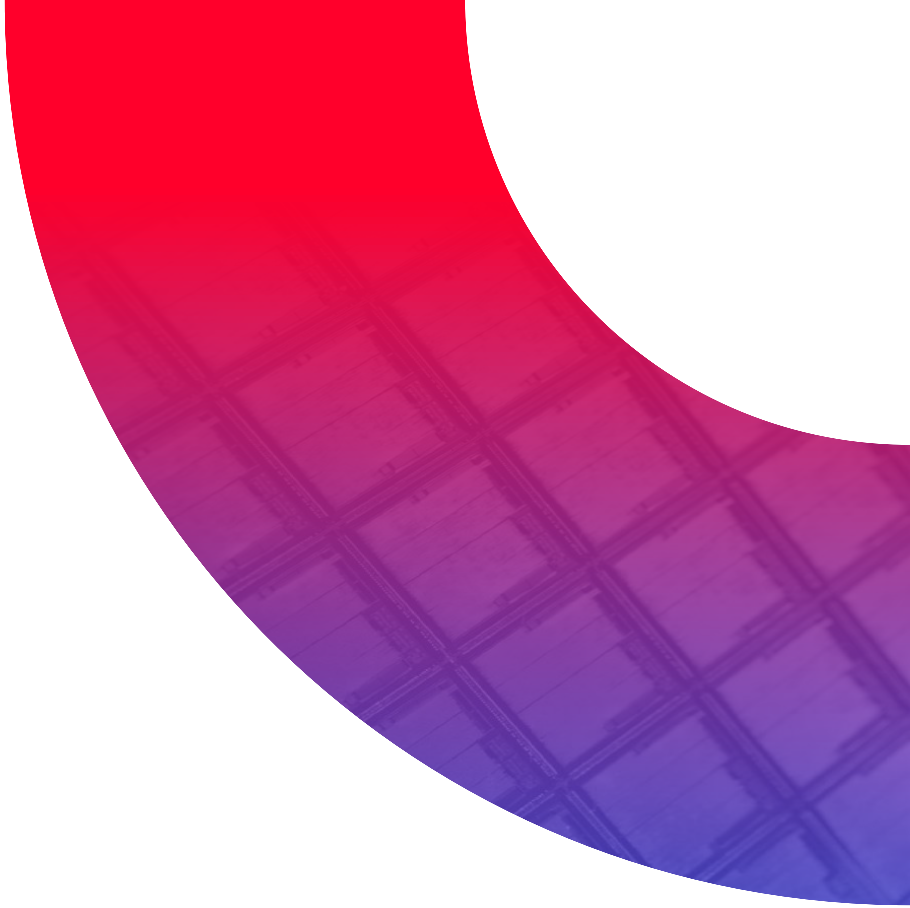


Simulations executed in Lumerical FDTD package

Wavelengths in **IRCD** range interact uniquely, leading to **parameter decorrelation** and **CD profile metrology**

IRCD





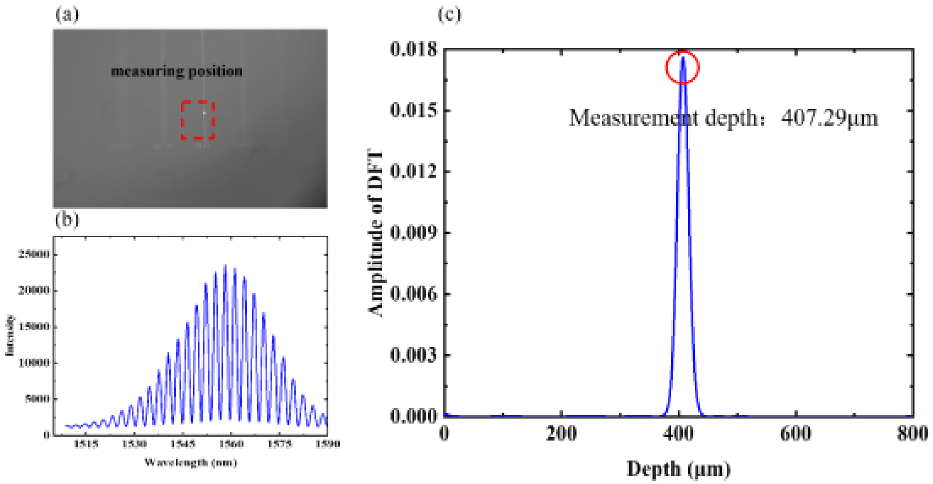
Simulation Study

Conventional OCD vs ICRD in Deep Trench Structures

Deep Trench Measurability

Conventional OCD vs IRCD

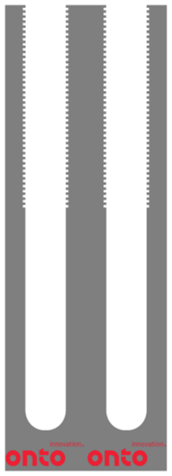
- Trench Depth
  - Normal Incidence Reflectometry capable of measuring beyond 400um depth
    - Utilizing near collimated light and NIR wavelength range
  - FFT algorithm used for depth extraction



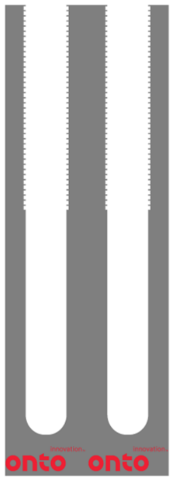
Wang, Z., Bai, C., Sun, X. & Hu, C. Optical method for depth measurement of high aspect ratio 3D microstructure. in *Optical Metrology and Inspection for Industrial Applications X* (eds. Han, S., Ehret, G. & Chen, B.) vol. 12769 1276909 (SPIE, 2023).

- Trench Sidewall Profile & BCD Challenges
  - Challenging with Conventional OCD technology due to spectra obfuscation from 2 sources:
    - Hard Mask
    - Sidewall Scalloping
      - Caused by DRIE process
  - Simulation Study
    - Structure Details
      - 4um Pitch, 2um CD, 20um Trench Depth
      - DOE
        - Hard Mask Thickness
        - Scalloping Amplitude @ 2 duty cycles
      - Conventional OCD vs IRCD

Deep Trench with SiO2 Hard Mask



Sidewall Scalloping 50% Duty Cycle

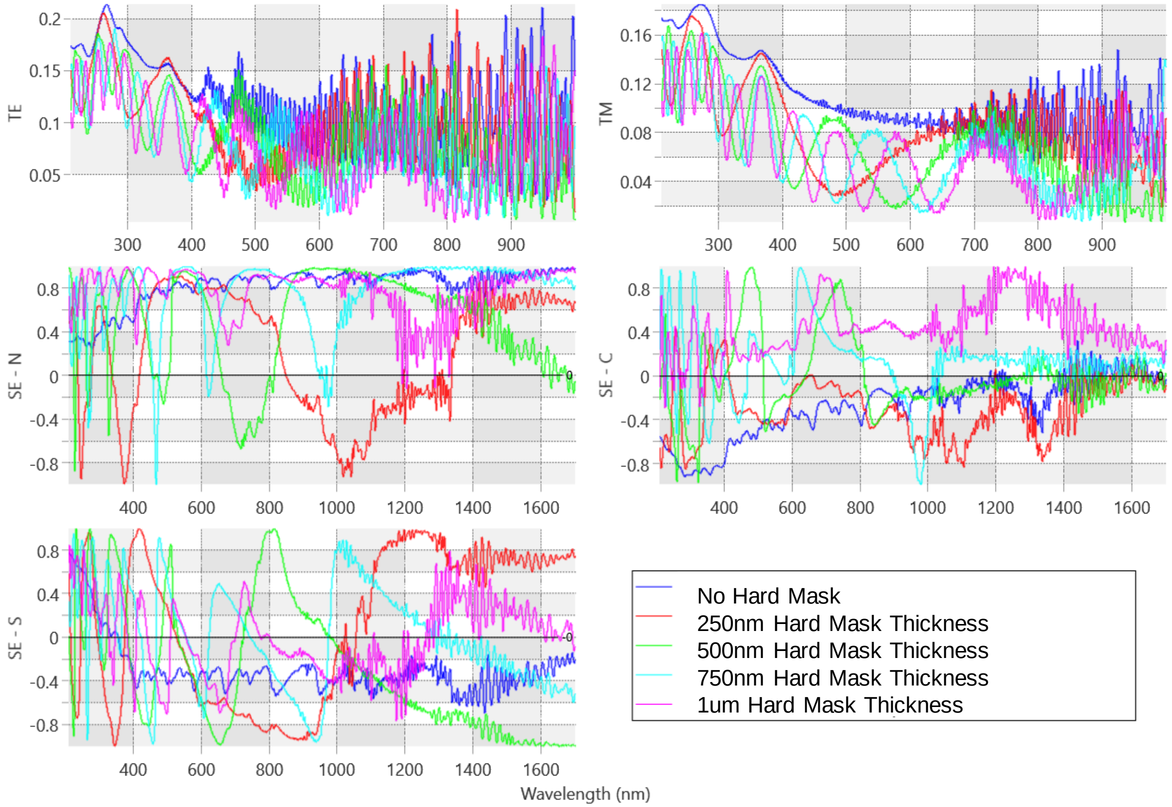


Sidewall Scalloping 25% Duty Cycle

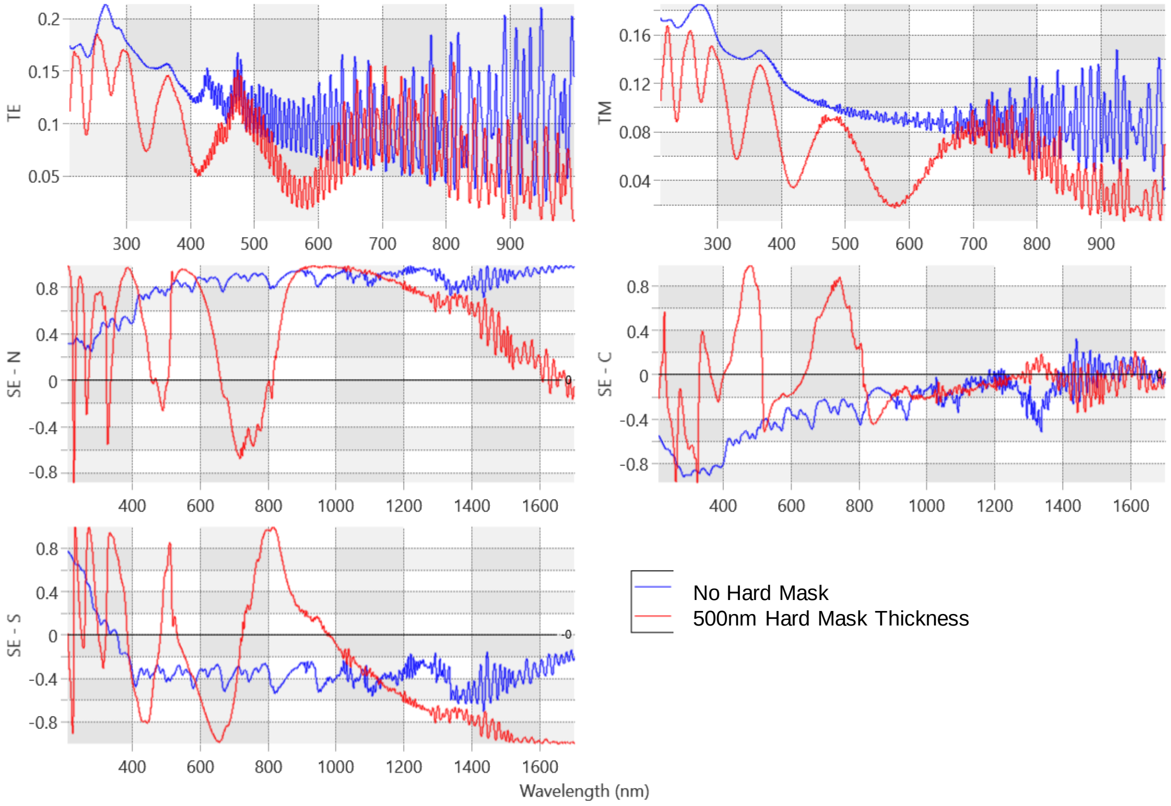
Hard Mask Thickness DOE Simulations

Conventional OCD Simulations

- Vary SiO2 Thickness 0-1000nm in 250nm steps



- SiO2 Thickness 0 & 500nm

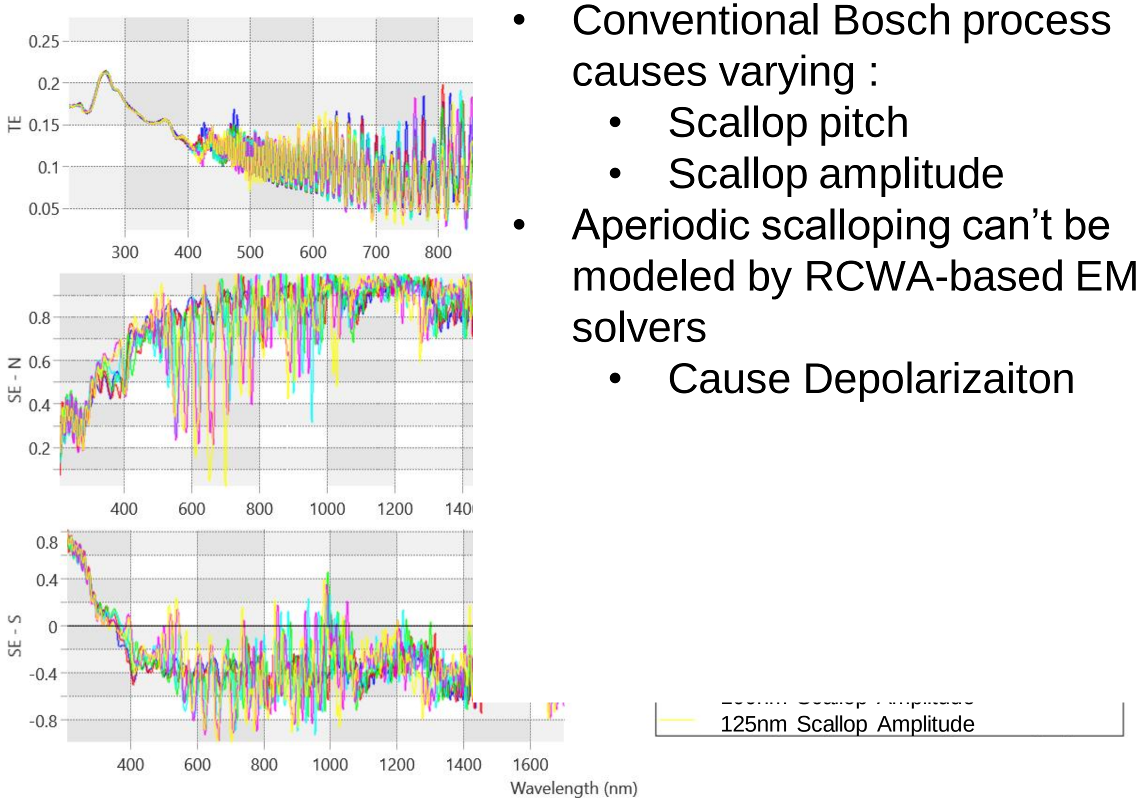


- Increasing hard mask thickness causes high amplitude, low frequency peaks
- Causes loss of sensitivity; more pronounced in the SE spectra

Sidewall Scalloping

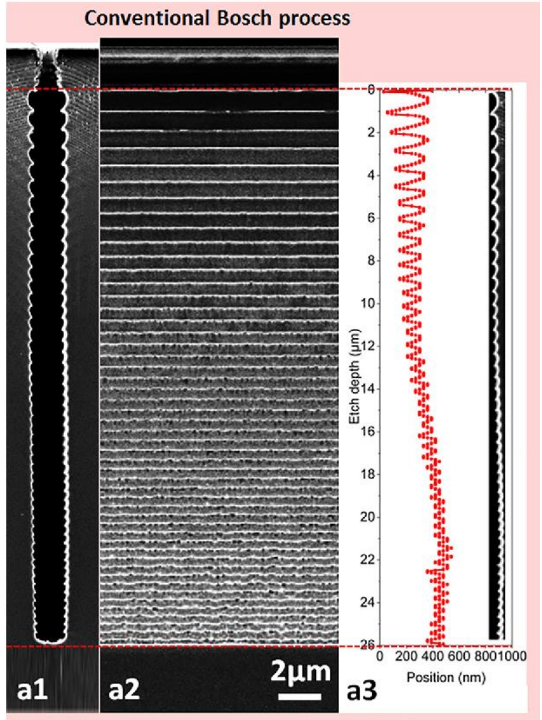
Conventional OCD Simulations

- Scallop: 0-125nm in 25nm steps @ 250nm Pitch & 50% Duty Cycle

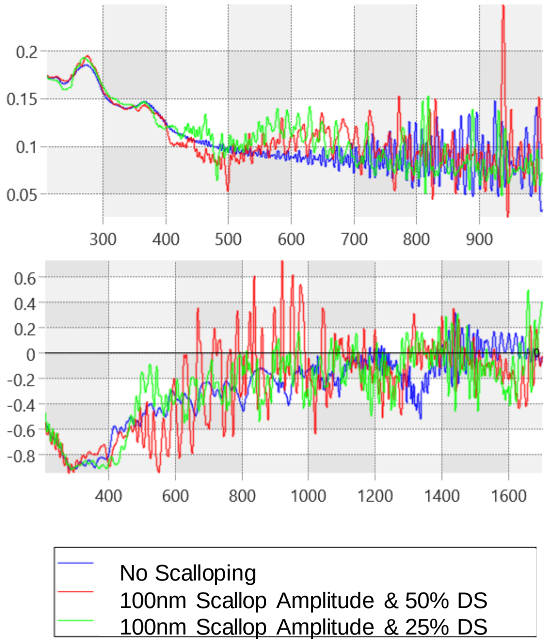


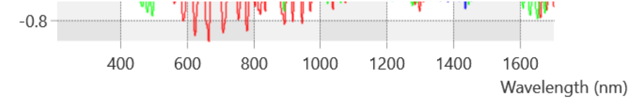
- Simulations are idealized
- Conventional Bosch process causes varying :
  - Scallop pitch
  - Scallop amplitude
- Aperiodic scalloping can't be modeled by RCWA-based EM solvers
  - Cause Depolarizaiton

- Scallop= 0 & Scallop=100nm Amplitude @ 250nm Pitch @ 50% & 25% Duty Cycle



Chang, B., et al.. DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process. *Microelectron Eng* **191**, 77–83 (2018).



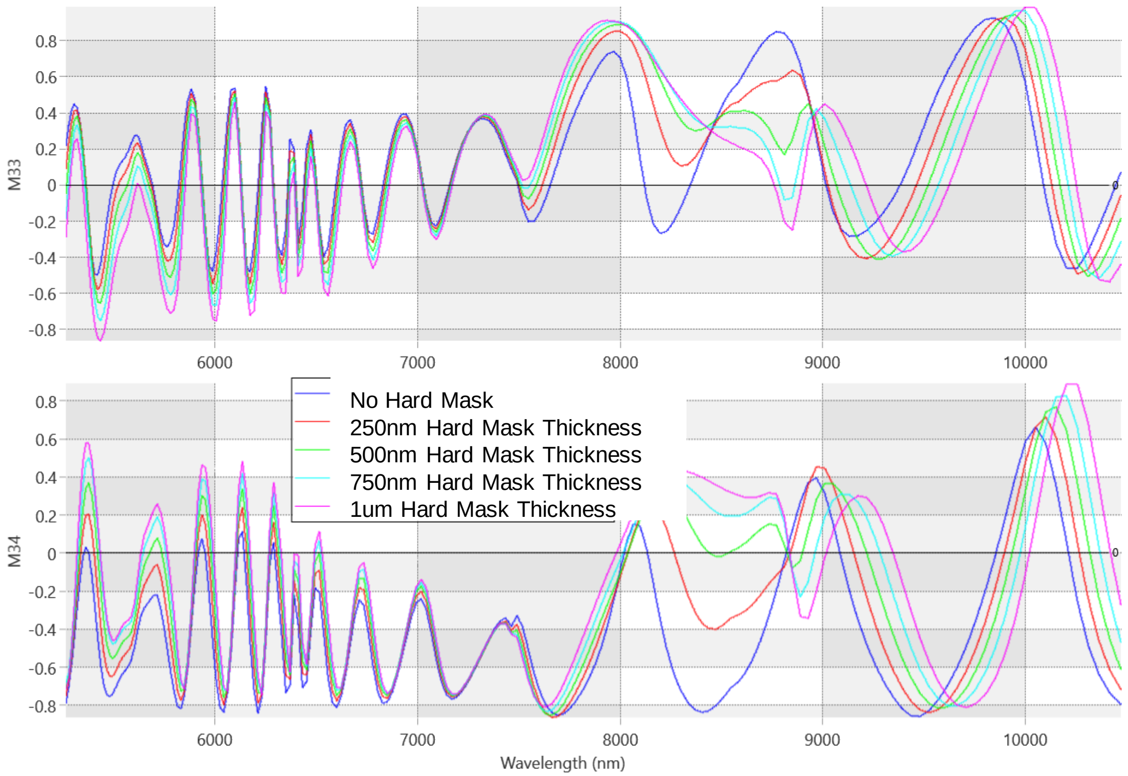


- Increasing scallop amplitude causes high amplitude, high frequency fringes
- Higher duty -> higher amplitude fringes

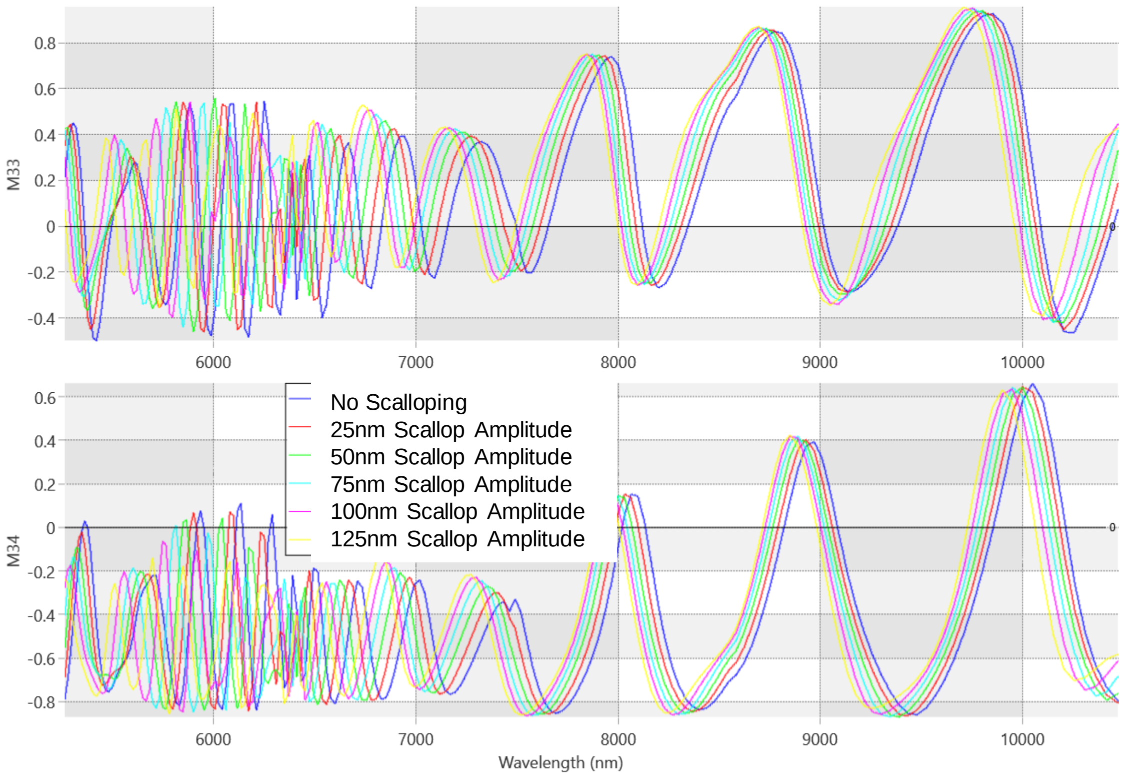
IRCD Simulations

IRCD

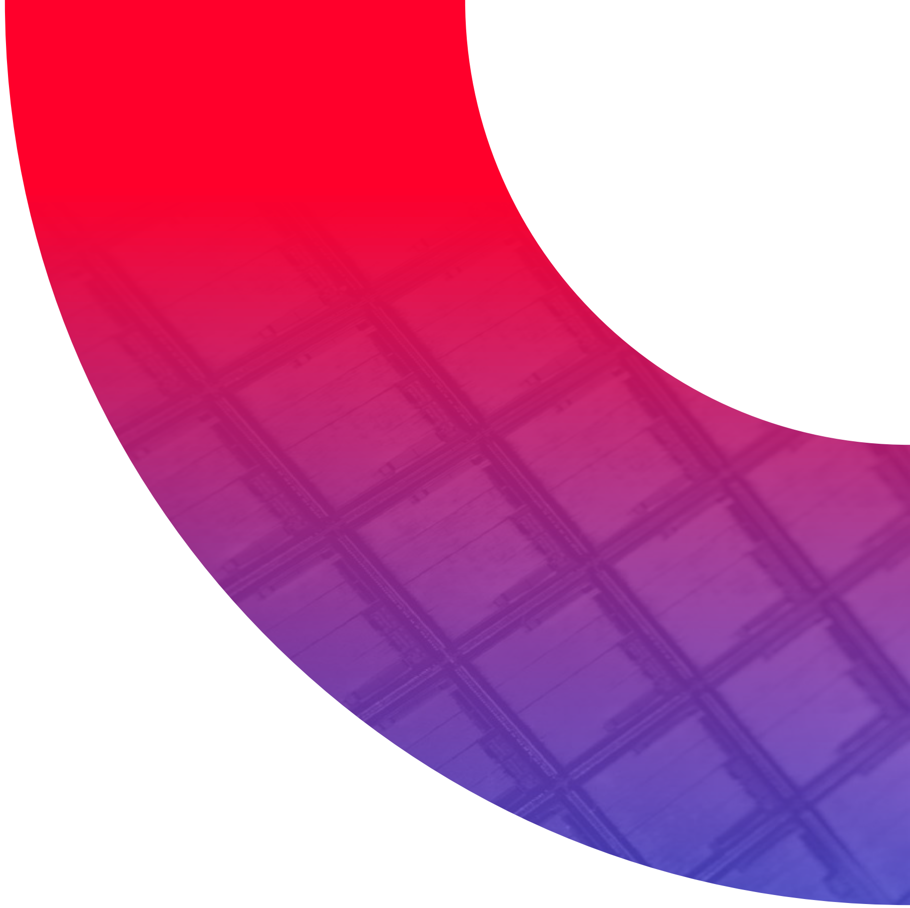
- Vary SiO2 Thickness 0-1000nm in 250nm steps



- Scallop: 0-125nm in 25nm steps @ 250nm Pitch & 50% Duty Cycle



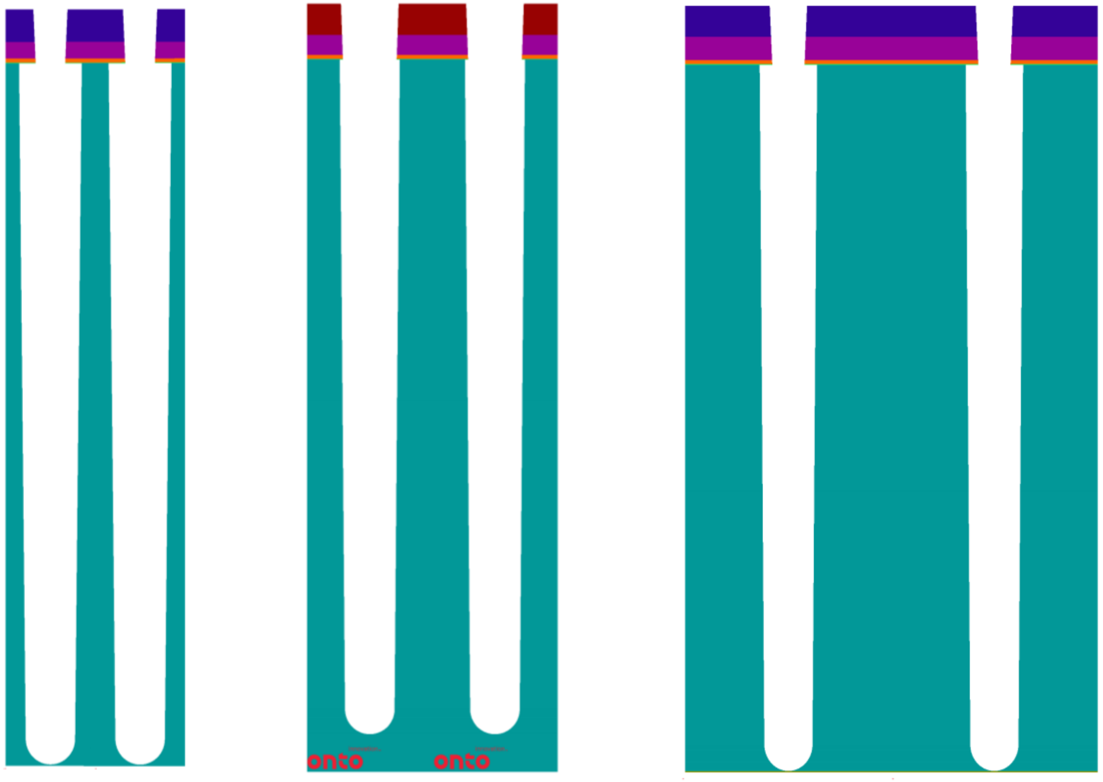
- Hard mask Simulation: attenuation only at SiO2 absorption band
- Scalloping Simulation: causes shift in spectra corresponding to average CD change



Experimental Results

Structure Details

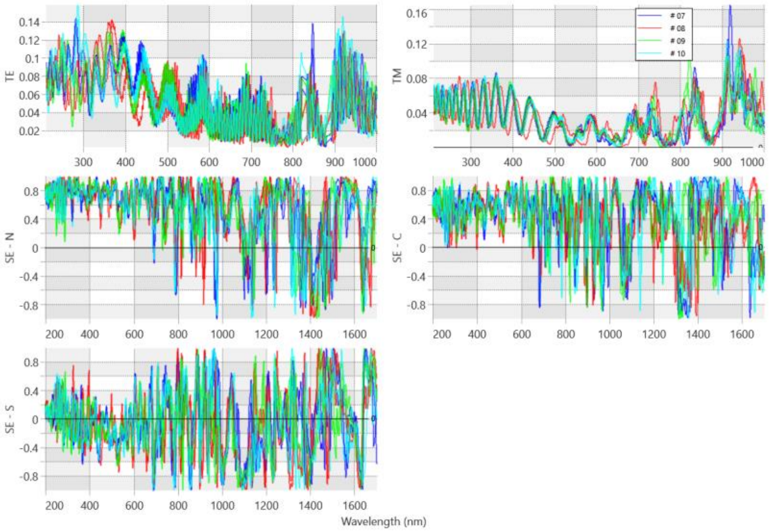
- DTI Post Trench Etch
- Structure Details
  - 3 Pitches (3.5um, 5um & 8um)
  - Nominal Trench CD = 2um
  - Nominal Depth = 30um
  - Hard Mask Film Stack
    - 1.2um SiO2/0.75um Poly-Si/0.2um SiN
  - Epi Layer = 20um lightly doped N Epi
  - Substrate = P++ doping
- DOE: SF6 Flow rate



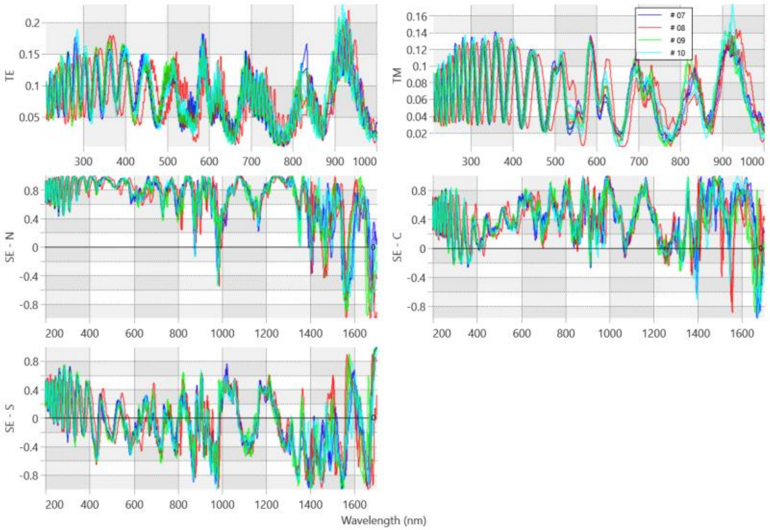
Spectral Analysis

Conventional OCD Spectra

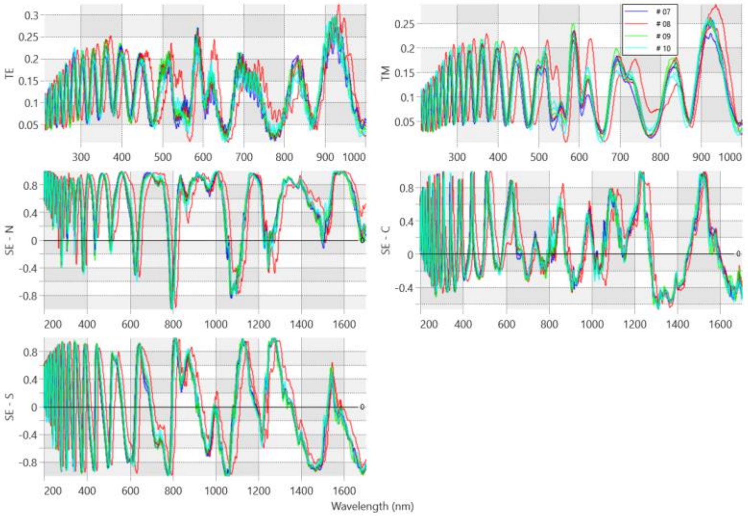
3.5um Pitch

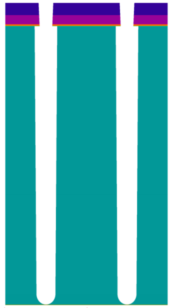


5um Pitch



8um Pitch





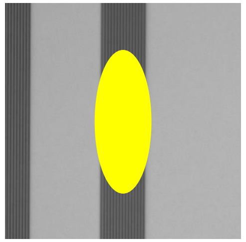
- Spectra exhibit characteristics of thick hard mask and scalloping
- Severity of scalloping decreases with pitch increase; hard mask is opposite

Spectral Analysis

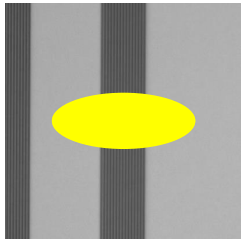
IRCD 0 & 90Deg Azimuth

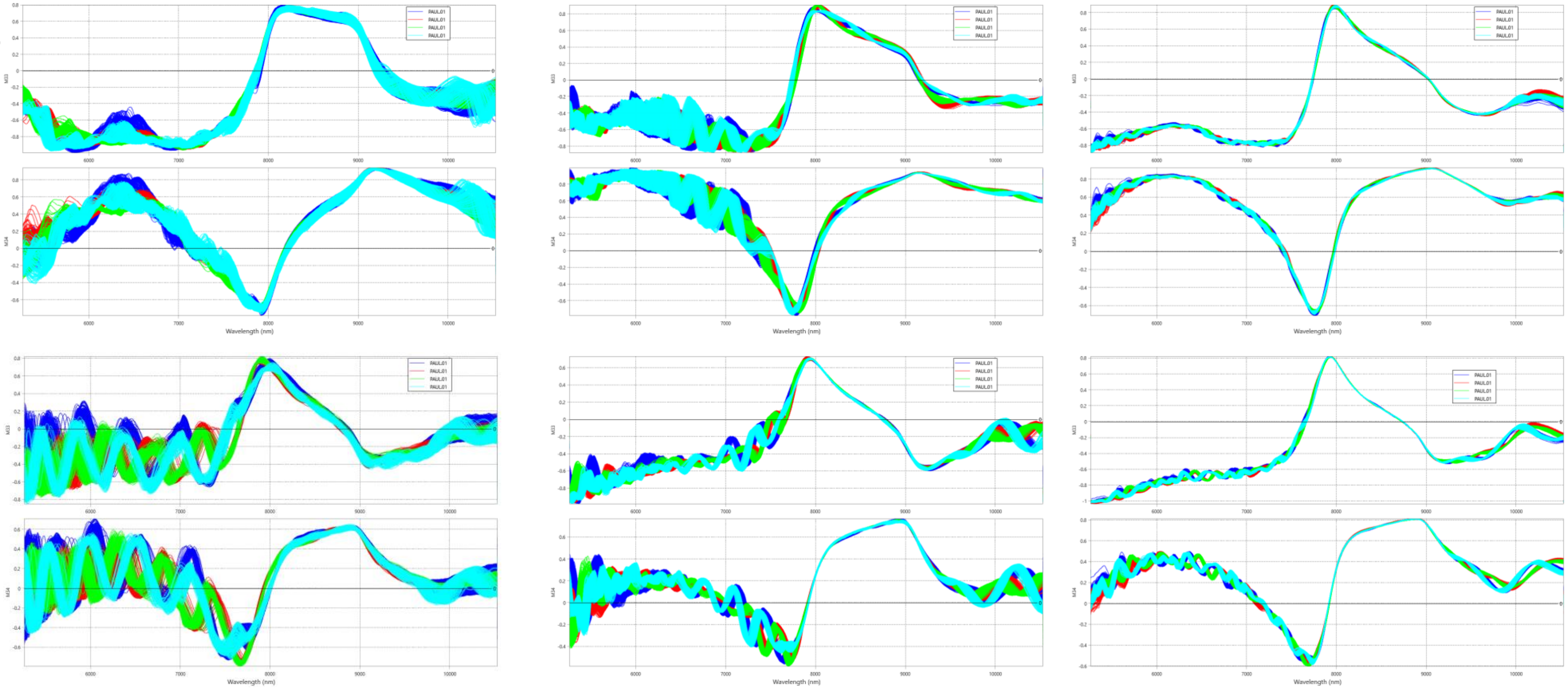
3.5um Pitch 5um Pitch 8um Pitch

90° (∥ Azimuth)



0° (⊥ Azimuth)

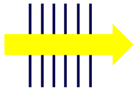
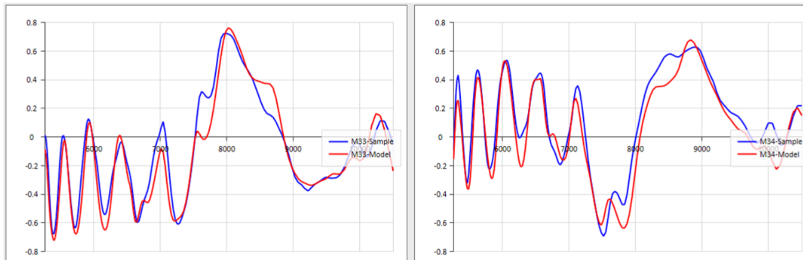
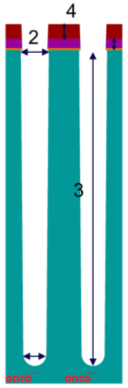
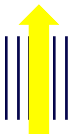
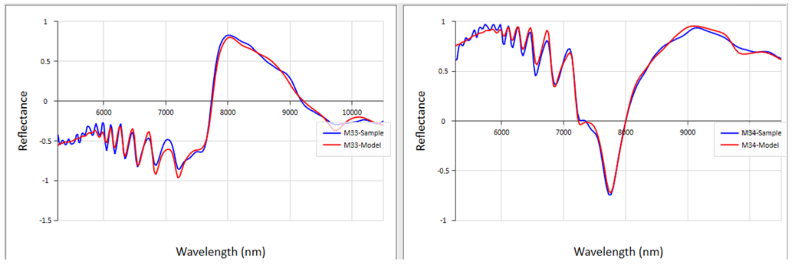
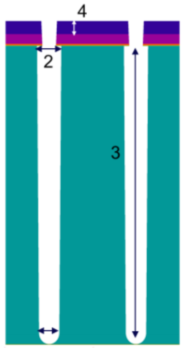
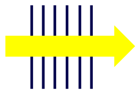
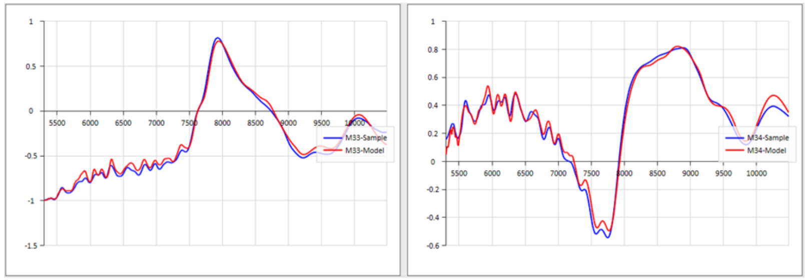




- Larger impact of Hard mask attenuation compared to simulations
- Perpendicular azimuth is more sensitive than parallel; but beam overfills

Model Details

- Floating Parameters
  1. DTI BCD (Key Parameter)
  2. DTI TCD
  3. DTI Depth
  4. SiO2 HM THK
- Fixed Parameters
  1. Si Undercut*
  2. Poly-Si THK

Structure	Azimuth	Model Fit to Experimental Spectra
		Model Fit to Experimental Spectra 
		Model Fit to Experimental Spectra 
		Model Fit to Experimental Spectra 

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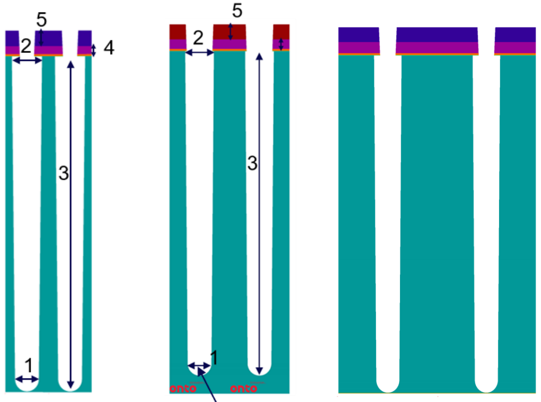
Set 1 Results

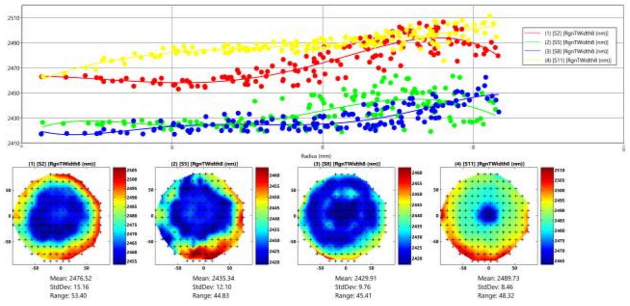
DTI Structures



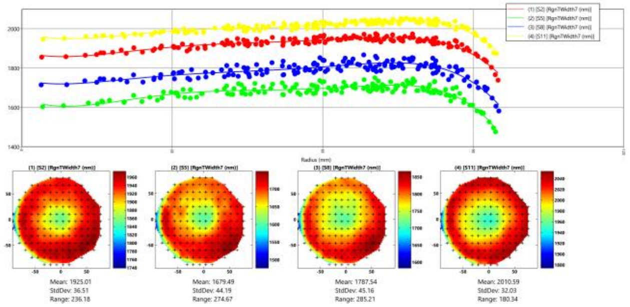
Key Parameter: BCD

3.5um Pitch

TCD

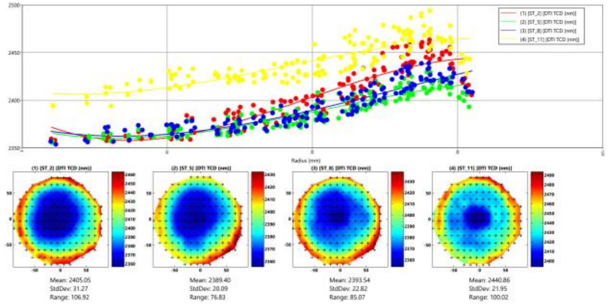


BCD

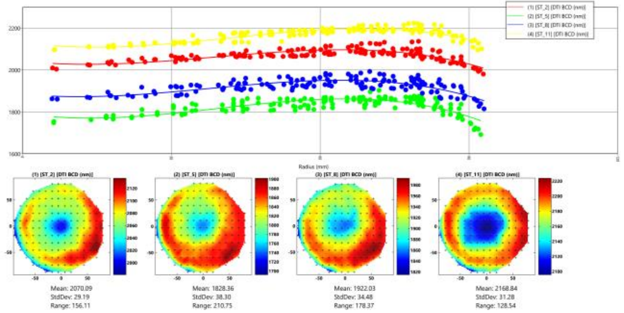


5um Pitch

TCD

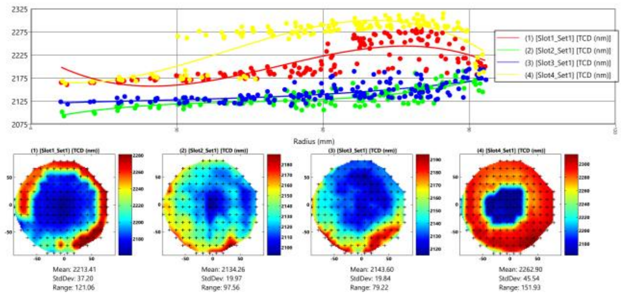


BCD

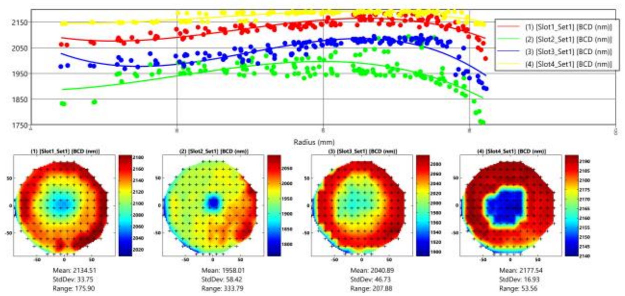


8um Pitch

TCD

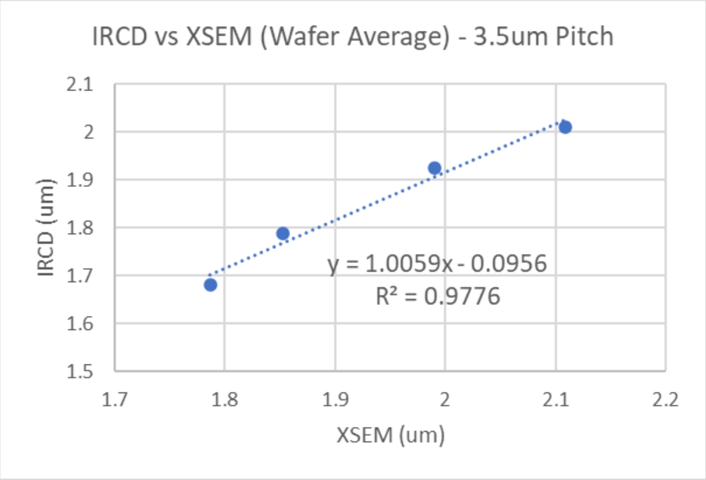


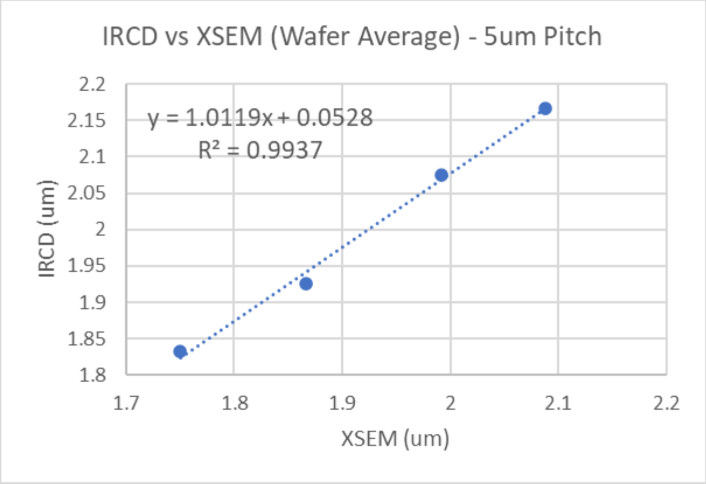
BCD

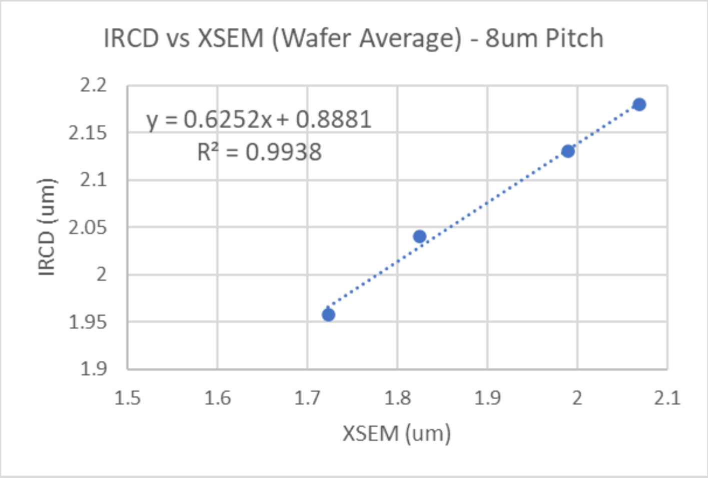


- IRCD shows clear BCD DOE & Decorrelation from TCD
- Sensitivity @ multiple pitches

Set 1 Results – Reference Correlation


IRCD vs XSEM (Wafer Average) - 3.5um Pitch


IRCD vs XSEM (Wafer Average) - 5um Pitch

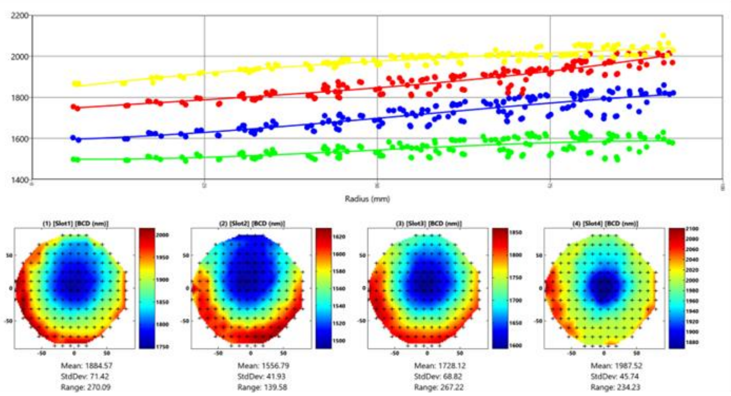

IRCD vs XSEM (Wafer Average) - 8um Pitch

- Excellent Wafer level correlation to XSEM
- 3.5um & 5um Pitch structures have slopes close to unity

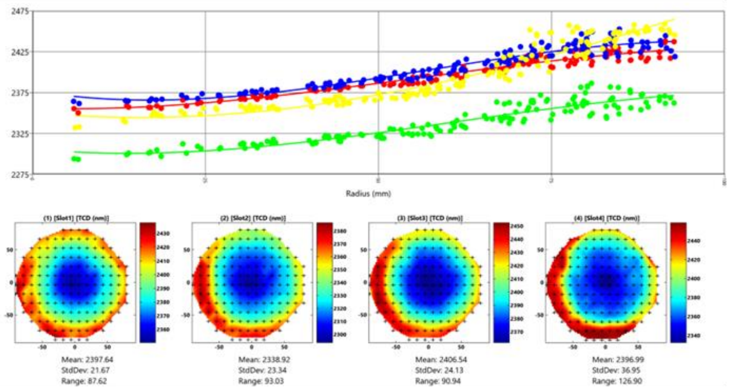
Set 2 Results

5um Pitch

BCD

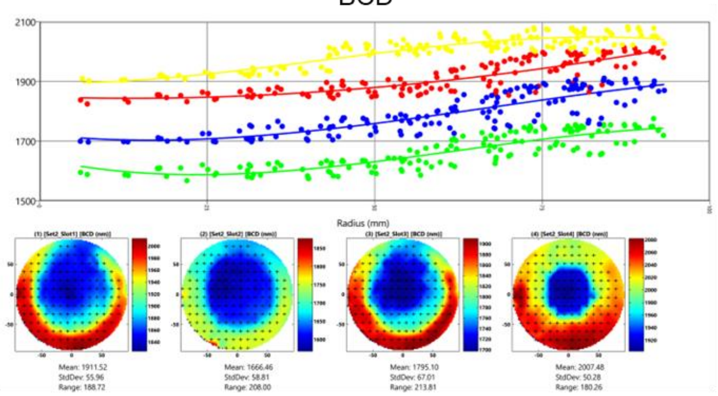


TCD

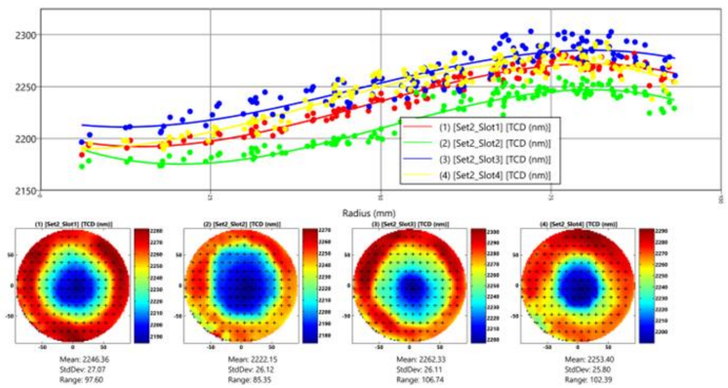


8um Pitch

BCD

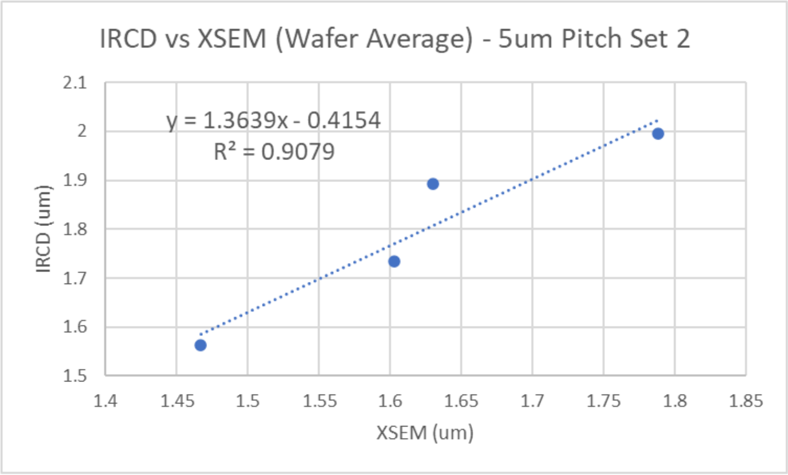


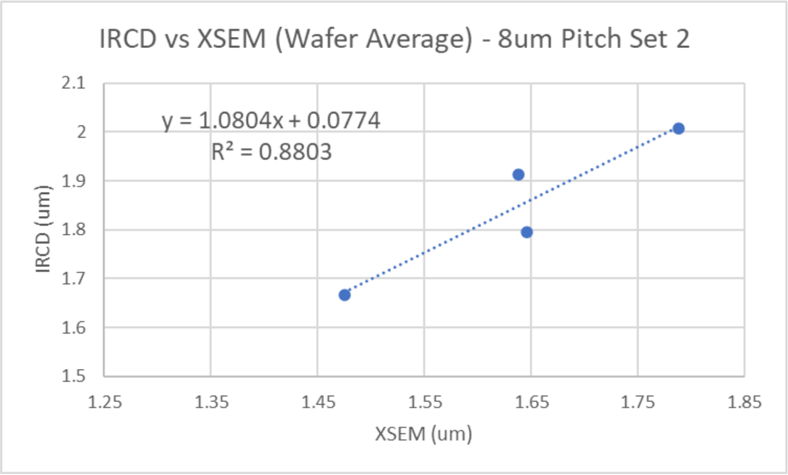
TCD



- IRCD shows clear BCD DOE & Decorrelation from TCD
- Similar DOE spacing

Set 2 Results – Reference Correlation





- Correlation drops but slope increases
- Reference performed on “sister” wafers; Reference investigation underway

Conclusion

- Deep Trench Isolation enables device scaling in BCD power management IC's & improves overall performance
  - Trench Depth is a critical parameter to measure in "typical" DTI
  - DTI process was developed to eliminate floating gate by adding substrate connection
    - Critical parameter to measure becomes the Trench BCD
- Simulation Study
  - Conventional OCD (UV-VIS-NIR) has challenges measuring DTI sidewall profile due to hard mask and sidewall scalloping
  - IRCD isn't affected by those modeling non-idealities
- Experimental Results
  - DOE was performed by adjust SF6 flow rate to change the Trench BCD
  - IRCD able to capture intended DOE @ 3 different pitches
    - BCD is decorrelated from TCD