SWTW18-60

Modern Probe Card Analysis…
Addressing Emerging Needs Cost-Effectively

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Introduction

Advances in semiconductor and test technologies have conspired to pose new challenges to probe card and probe card analyzer suppliers and their customers.

This session addresses those challenges and potential solutions.

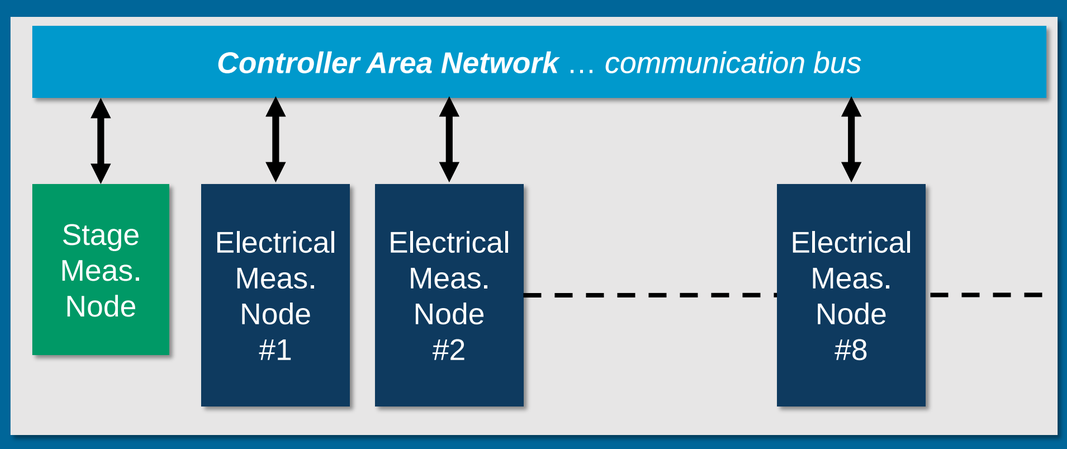
- **Scalable architecture delivers**
  - Higher channel counts
  - Flexible circuit and power control for enhanced test coverage
  - Enhanced throughput –modularity and parallelism
  - Electrical states for advanced debugging and repair
- **“Infinite plane” for Probe Card Interface expansion**

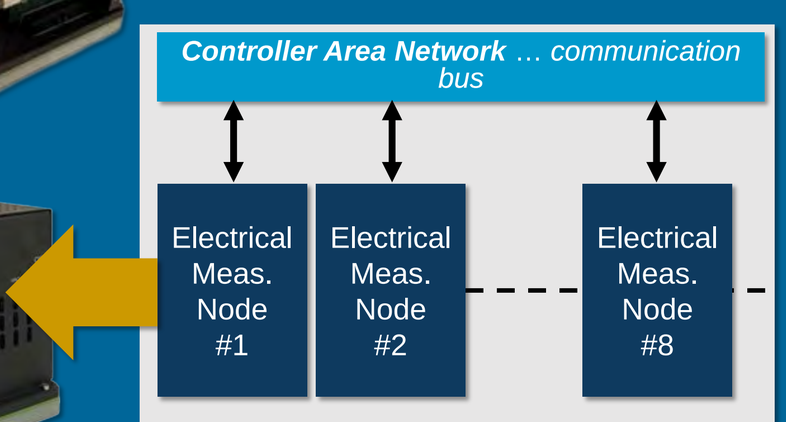
Scalable Architecture for Expansive Channel Counts

Challenge: Modern probe cards require higher channel counts and re-configurability.

Solution: Implement scalable design

- 14,400 channels ... scalable to market requirements.
- Electrical Measurement Nodes (EMNs) attach/detach from CAN bus as needed
- Electrical measurements taken directly by devices within EMN





Scalable Architecture for Expansive Channel Counts

Node Controller Board

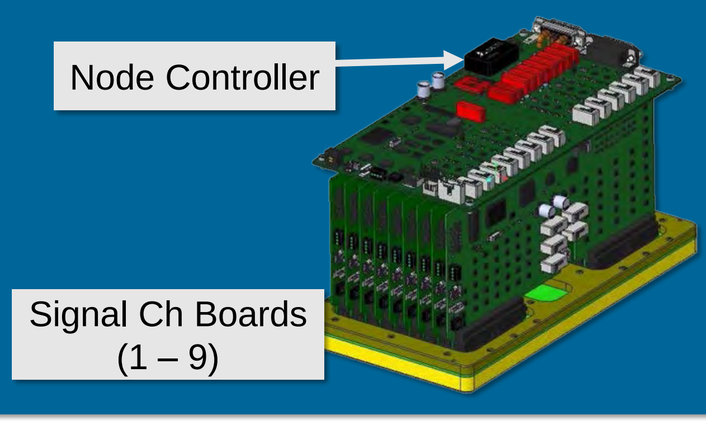
- Contains meters and programmable supplies
- Improved measurement fidelity
- Connections for external supply inputs (driven by state control)

Signal Channel Boards (1-9)

- Standard signal measurement channels or low current utility channels

Utility Channel Board

- Low and expanded high current capable utility channels

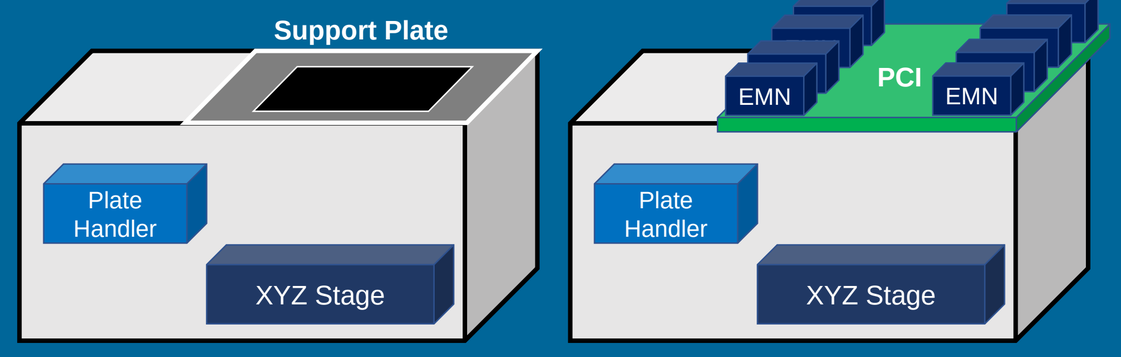


“Infinite Plane” Architecture

Challenge: Protect Probe Card Interface investment.

Solution: Implement an Infinite Plane architecture.

- Legacy compatibility as well as large expansion in X, Y, and Z



Flexible Power and Circuit Control – Enhanced Test Coverage

Challenge: Probe card designs require multiple power supplies

Solution: Multiple programmable supplies.

- Connection to industry standard voltage levels via programmable supplies
- Current limit can also be set for the programmable supplies

External Port Connection

- Connect to an external port allowing for an external device connection (power supply, meter, etc.)
- Driven from within the probe card’s state definition

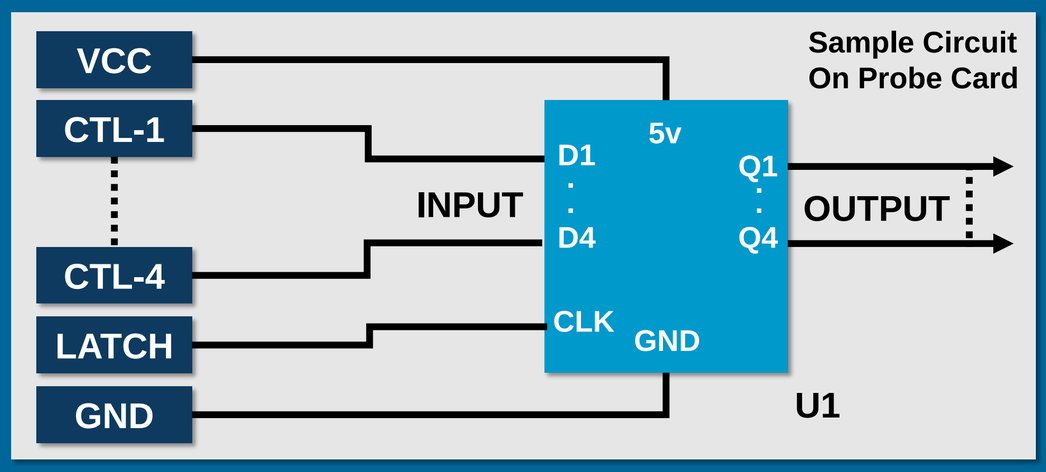
Enhanced Circuit Control Within Probe Card Definition

Challenge: Advanced probe card electrical designs require enhanced circuit control to expand test coverage.

Solution: Analyzer supports state definition and activation during probe card test.

Example: Sample circuit on probe card requires sequencing four bit input (D1-D4) from 0 to F (HEX) to drive output and corresponding circuitry.

- Generate entries in probe card state definition to establish power connections and perform logic actions
- Once a state is defined, it can be assigned to specific probes and/or components
- State will be activated when testing these specific probes and/or components. State can also be activated manually while in debug mode.



Steps to generate state definition for sample circuit on probe card.

Define Power State:
VCC, GND

↓

Define Control Line Inputs:
CTL - 1, 2, 3, 4

↓

Define Clock Input:
LATCH

↓

Define Logic State to Sequence Input from:
0 to F

↓

Assign State:
Probe, Component, Global

Debugging and Repairing Electrical State Issues – Stepping Through Defined States

Challenge: Must validate and troubleshoot advanced circuits on probe card.

Solution: Enhanced circuit control provides sequenced definitions allowing for active 'step-mode' debugging.

Example: Corresponding devices/circuitry connected to output of U1 are not functioning properly thus need to actively troubleshoot input/output conditions.

- Operator can step through state definition's power and logic entries as desired and verify circuit input/output conditions

Debugging and Repairing Electrical State Issues – Stepping Through Defined States

- Input and output test points can be monitored while stepping through defined state actions.
- Power supply current draw will also be monitored during state activation triggering fault conditions when exceeding established current limits

Step through defined Power State that connects:
VCC, GND

↓

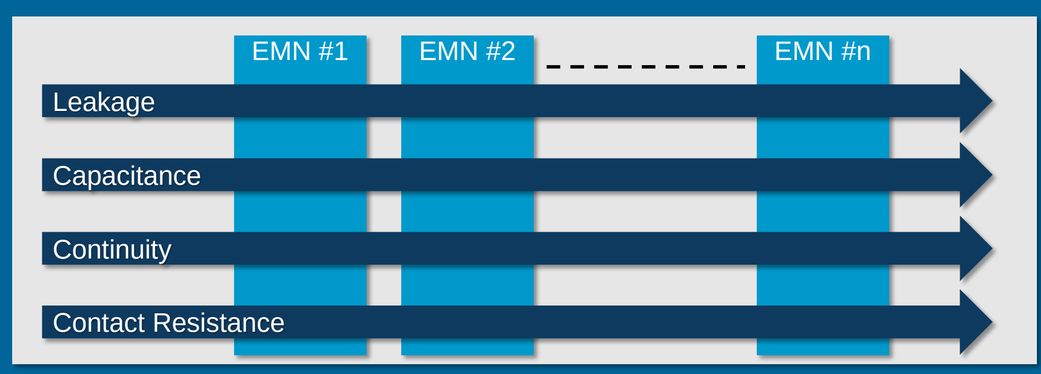
Step through defined Logic State that sequences input from: **0 to F**

Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Advanced probe cards require an extensive suite of electrical tests to achieve acceptable test coverage.

Solution: Scalable analyzer architecture supports many electrical test measurements in parallel.

With each Electrical Measurement Node (EMN) having independent meters, electrical measurements are performed in parallel across nodes when possible.

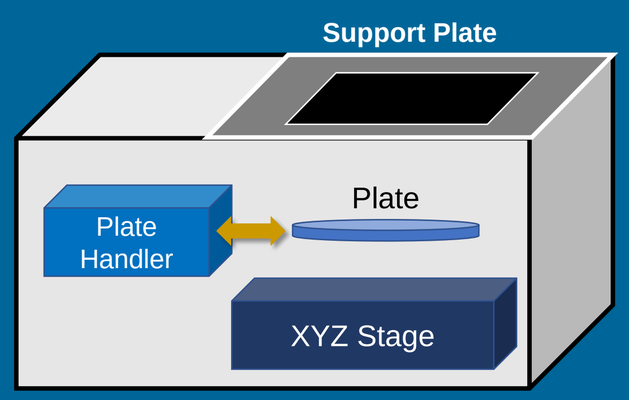


Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Tests of advanced probe cards require manual user interaction with system during active test.

Solution: Optimize automation of analyzer; implement automated plate handling.

- Accessory plates will be loaded/unloaded automatically during test (cleaning, contact resistance, leakage at overtravel, etc.)
- Accessory plate size allows for single touchdown of entire array during test
- Accessory plate loading/unloading does not compromise probe card or PCI placement thus optimizing productivity/stability/repeatability

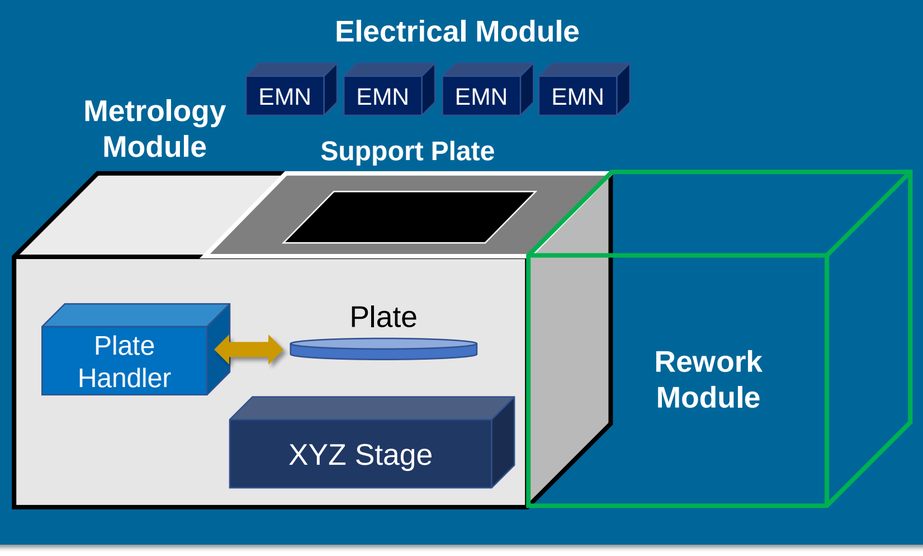


Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Advanced probe cards require incremental (and more advanced) testing to validate performance. This must be delivered cost effectively.

Solution: Analyzer architecture must be modular to support flexible requirements; the architecture must be cost-effective.

- Metrology with automated plate handling
  - Stage components for testing planarity, alignment, contact resistance, cleaning
- Electrical
  - Electrical measurement system for testing leakage, capacitance, confirming bussed channels, detecting shorted channels, capacitor/resistor measurements, enhanced circuit control
- Rework
  - Provide capability for probe-side access

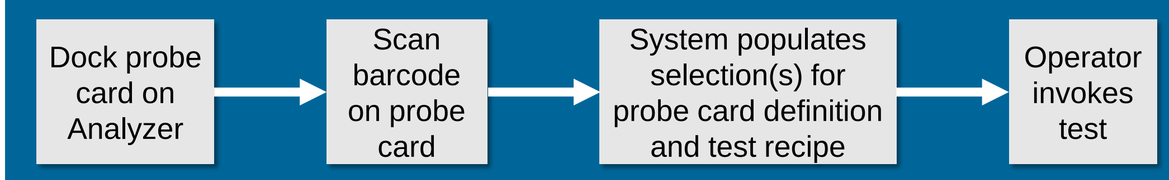


Process Control – Probe Card ID

Challenge: Probe and probe card manufacturing floors increasingly support multiple probe card technologies. Recipe management becomes complex driving the need for process control.

Solution: Drive card/recipe selections using barcode identifier on probe card.

- The number of selections presented will be controlled based on configured mode (multiple or golden single)
- This flow is similar to the SECS/GEM mode of controlled card/recipe selection

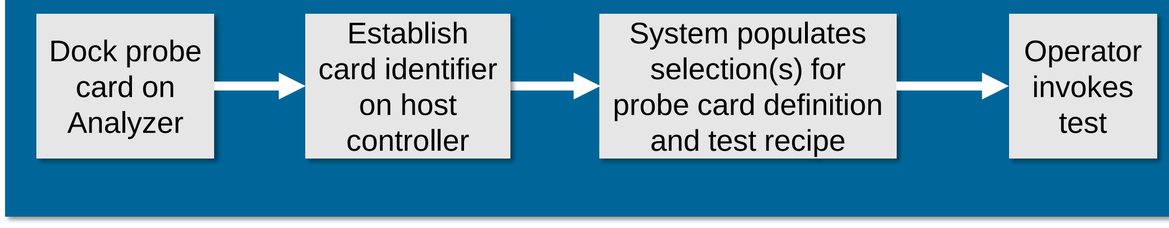


Process Control – SECS/GEM

Challenge: Incremental probe card manufacturing and probe floor complexity drive the need for process control and reporting of tool status.

Solution: Provide SECS/GEM capability.

- Controlled card/recipe selection via host controller (similar to barcode driven test)
- System status mode and requests: remote/local, idle/processing/running, up/down time
- Alarm event reporting, handling, and logging

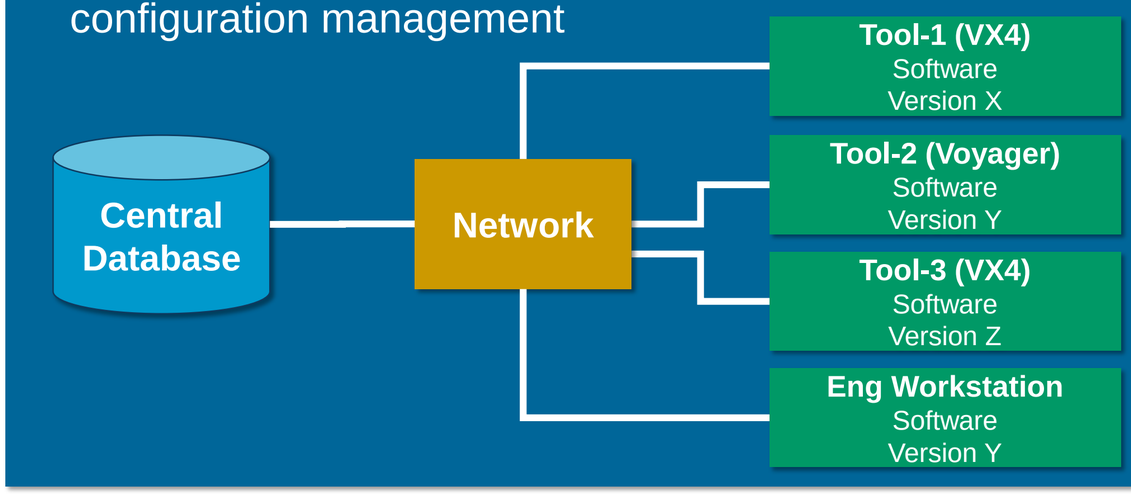


Centralizing Database – Flexibility

Challenge: Probe and probe card manufacturing floors increasingly support multiple generations of probe card technology and analyzer capability. Recipe and software revision management becomes complex.

Solution: Implement flexible database design so that analyzers are not required to run same software version.

- Tools running different software versions are able to share same database
- Card and recipe definition versions managed by tool and database
- Centralized database also allows for remote tool configuration management

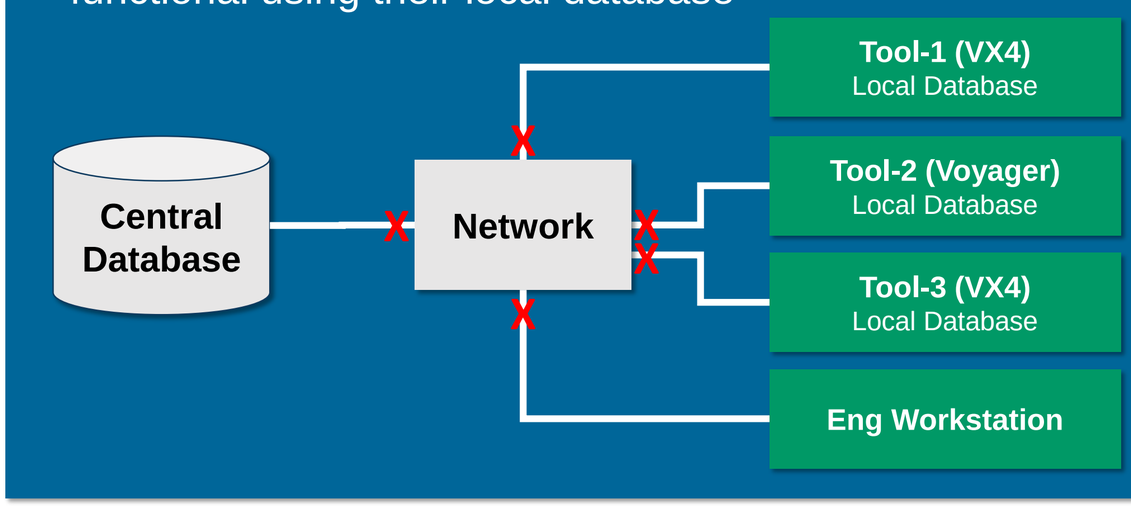


Centralizing Database – Fault Tolerance

Challenge: Fluctuations in power source or network availability disrupt manufacturing process.

Solution: Implement fault tolerant distributed database design.

- Local database used as primary source
- Local and centralized database are synchronized
- If centralized database or network go down, tools are still functional using their local database



Summary

This paper addressed some of the new challenges and potential solutions to probe card and probe card analyzer suppliers and their customers.

- Scalable architecture for expansive channel counts
- Infinite Plane architecture supports Probe Card Interface flexibility
- Flexible power and circuit control for enhanced test coverage
- Parallelism and Test Modularity deliver throughput improvements

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