Large-field, fine-resolution lithography enables next-generation panel-level packaging

By John Chang [Onto Innovation]

Rapidly growing demand for new types of functionality across an expanding range of applications, including 5G communication, smartphones, data centers, servers, high-performance computing (HPC), artificial intelligence (AI) and the Internet of Things (IoT), is driving a fundamental shift in the way electronic devices are designed and manufactured. Gone are the days when advances were defined by an increasing number of shrinking transistors with ever-faster switching times and lower power consumption, all fabricated as a single, monolithic integrated circuit (IC). Many of today's most advanced systems integrate multiple die, each optimized for a specific capability and fabricated with a process designed specifically for that type of circuit. These disparate chips are then connected using advanced packaging (AP) technologies, a process known as heterogeneous integration (HI) (**Figure 1**).

One example of HI uses advanced IC substrates (AICS) in a process known as ultra-high density (UHD) panel fan-out. This fan-out panel-level process (FOPLP) is a redistribution lines (RDL)-first approach, where many layers of patterned conductive and insulating material are processed on both sides of a large panel to route electrical signals between the integrated chips, which are added last. Once the RDL layers are complete, solder bumps are added to form connection points that will mate with matching connection pads on the component ICs. Package substrate sizes are expected to reach 150mm x 150mm in the next few years. Panels, which may be 500mm x 500mm or larger, can accommodate many more packages per panel than the substrates used in wafer-level processes, which are restricted to round, wafer-like substrates of 300mm or less in diameter (**Figure 2**).

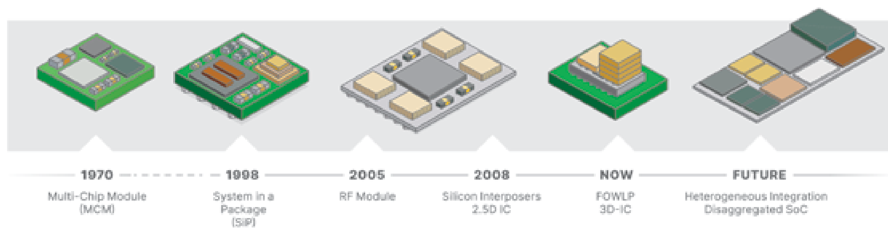


Figure 1: Heterogeneous integration enables next-generation device performance gains by combining multiple silicon nodes and designs inside one package. The package size is expected to grow significantly. SOURCE: Cadence

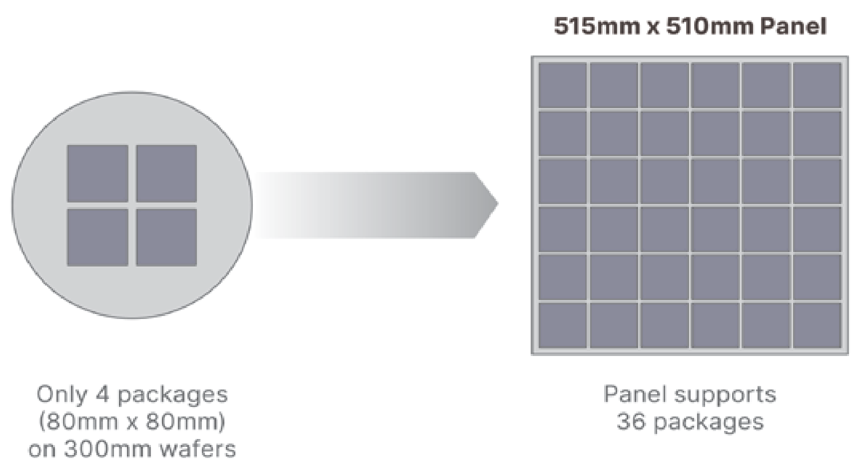


Figure 2: The number of 80mm x 80mm packages that fit on a 300mm wafer compared with the number of 80mm x 80mm packages that fit on a 515mm x 510mm panel.

The lithography challenge for large heterogeneous integration is the limited size of the exposure field (typically 60mm x 60mm or less) for most currently available lithography systems. Smaller-field systems can be used to pattern large substrates by stitching together multiple exposures, but this affects both productivity and yield because of the need for multiple exposures of multiple reticles and the risk of errors at the stitching boundaries. A large exposure field would eliminate these impediments. However, there are also challenges associated with a large exposure field. These include panel warpage and distortion, which can impact critical dimensions, uniformity and overlay.

We describe here the use of our large-field lithography system (JetStep® X500) to expose 250mm x 250mm substrates in a single shot on 515mm x 510mm panels. Our evaluation included: 1) critical dimension (CD) control for 3µm, 5µm and 6µm lines/spaces, and 15µm and 20µm vias; 2) CD uniformity across the exposure field; and 3) overlay accuracy. We used copper clad laminate (CCL) and Anjinomoto build-up film (ABF) panels for resolution, and glass panels with liquid resist for overlay and uniformity. The large field eliminates stitching, allows the exposure of more large package substrates in a single shot and requires fewer shots to complete a panel. **Figure 3** compares the exposure layout for a large field (250mm x 250mm)

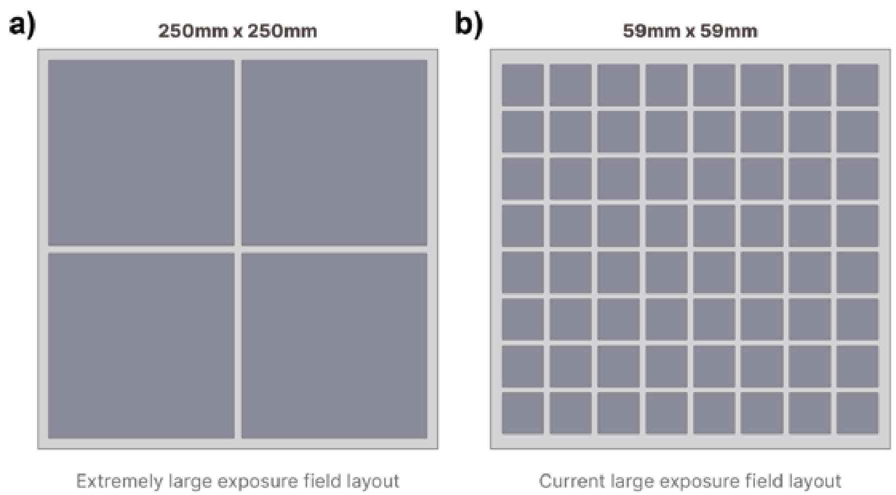


Figure 3: a) (left) The exposure layout for a 515mm x 510mm panel using a large exposure field (250mm x 250mm) compared with b) (right) the exposure layout of a smaller field (59mm x 59mm).

and a smaller field (59mm x 59mm) on a 510mm x 515mm panel. With the large exposure field, the panel can be completely exposed with just four shots, while the smaller field requires 64 shots.

Lithography system

The increased topological variation expected for larger panels, physical distortion during the RDL build-up process and the greater feature heights typical of RDL all contribute to the requirement for more depth of focus (DOF) in the pattern projecting optics. In any optical system, DOF and resolution are inversely related, i.e., gains in resolution require sacrifices in DOF and vice versa. Resolution and DOF are related through the system's numerical aperture, as shown in **Equation 1** and **Equation 2**. With feature sizes in the micrometer range, the resolution requirements for advanced packaging and advanced IC substrates are less demanding than requirements for front-end lithography, where feature sizes are 1,000 times smaller. At the same time, the use of thicker resist films and larger variations in substrate topography require greater DOF. The projection optics of the lithography system used in this demonstration were designed with a lower numerical aperture to meet both the resolution and DOF requirements of the application.

$$R = k1\lambda / N.A. \quad \textbf{Eq. 1}$$
$$DOF = k2\lambda / N.A.^2 \quad \textbf{Eq. 2}$$

Where k1 and k2 are process factors, and λ is wavelength.

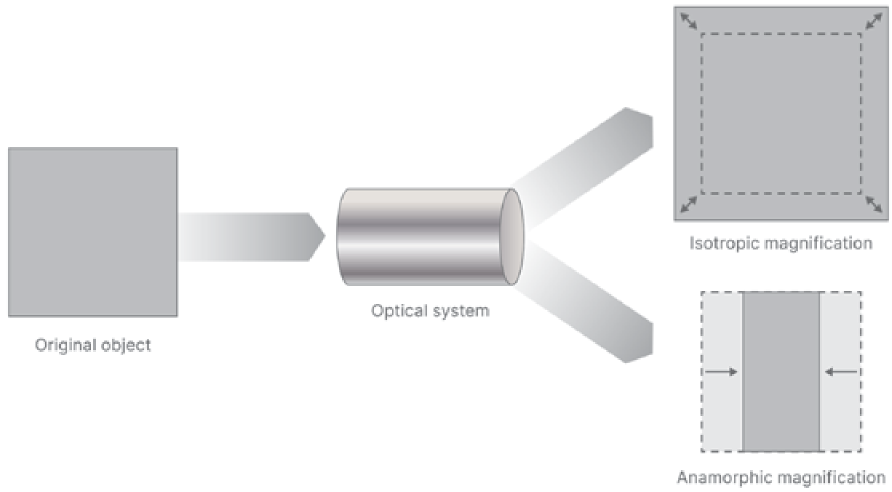


Figure 4: Isotropic magnification and anamorphic magnification compensation.

The system's 2.2x magnification projection lens enables up to a 250mm x 250mm exposure field size, with 3µm line/space resolution, ±400ppm magnification compensation and ±100ppm anamorphic magnification compensation, with overlay accuracy better than 1µm.

Low lens distortion and accurate step and settle movement are also key to meeting the overlay and uniformity requirements. Distortion in this system is less than 1µm across the 250mm exposure field. The system's stage is driven by 8 motors to ensure accurate step and settle behavior, even when loaded with the weight of the large panel.

During the FOPLP substrate build process, many layers of RDL and ABF are added to the panel. These films distort the panel in the X axis, Y axis and Z axis during thermal cycling. Magnification compensation allows the system to accommodate these changes in the substrate. Two kinds of compensation are needed. Isotropic magnification shrinks or enlarges the pattern equally in all directions. Anamorphic magnification enlarges or shrinks the patterns anisotropically to correct for distorted panel registration errors. Both adjustments are necessary to achieve good overlay and maintain high package yields. **Figure 4** shows the difference between isotropic magnification and anamorphic magnification.

Resolution

The large-field lithography system was evaluated for CD control of lines/spaces and vias, CD uniformity, and overlay.

3µm lines. Figure 5 shows the results of the 3µm line/space resolution evaluation. A CCL/ABF substrate with a 10µm-thick dry film resist was selected for this demonstration, resulting in lines with just over a 1:3 aspect ratio. Best dose and best focus were determined using a focus exposure matrix (FEM). Best dose was used for the resolution demonstration. The figure indicates that CDs showed less than 10% deviation from -10µm to -70µm, at a DOF of 60µm. The data from the FEM were used to generate a Bossung plot (**Figure 5a**) in which the X-axis is focus (µm) and the Y-axis is CD (µm). The plot shows the 60µm DOF. **Figure 5b** also includes a lower magnification

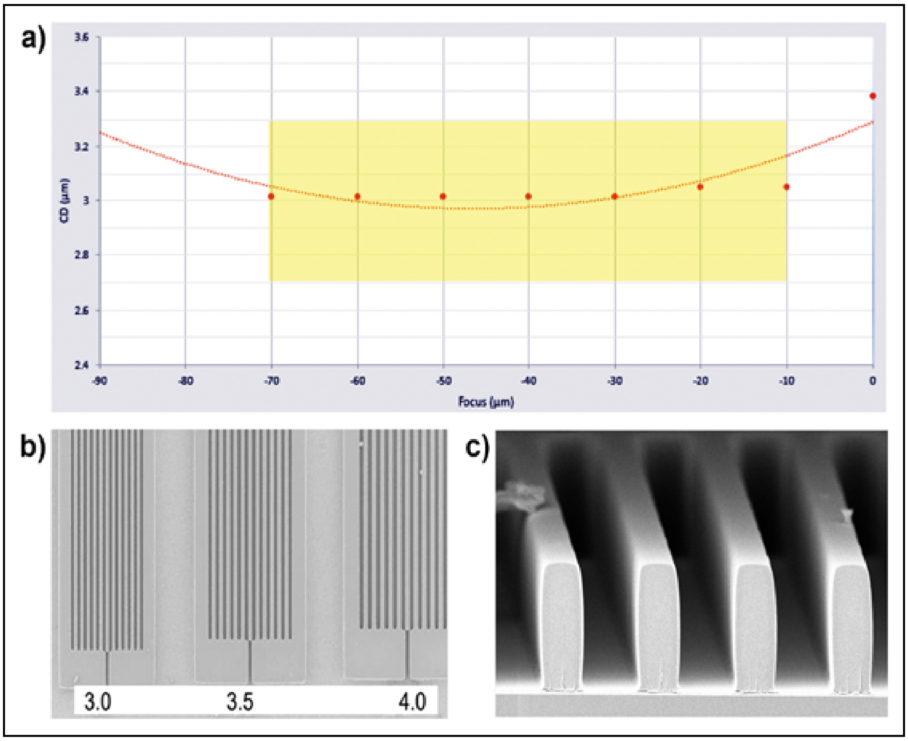


Figure 5: a) Bossung plot generated from FEM data showing less than 10% deviation over 60µm DOF; b) Lower resolution image of 3µm, 3.5µm and 4µm isolated and dense area line/space arrays; c) Cross-section image of 3µm lines in 10µm thick dry film resist on copper substrate; the line critical dimension is 3.181µm, and the resist height is 9.873µm in the cross-sectional image.

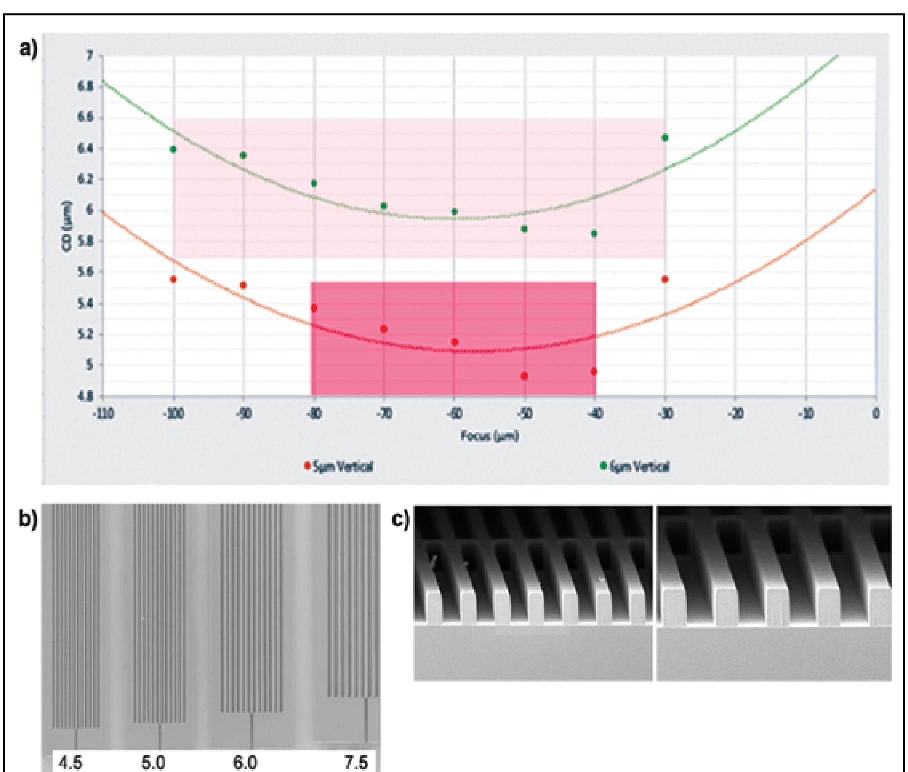


Figure 6: a) Bossung plot generated from FEM data showing less than 10% deviation over 40µm DOF for 5µm lines and 70µm DOF for 6µm lines. b) Lower resolution image of 4.5µm, 5µm, 6µm and 7.5µm isolated and dense area line/space arrays. c) Higher resolution cross-sectional images of 5µm and 6µm lines in a 10µm-thick dry resist on copper substrate.

image of 3µm, 3.5µm and 4µm isolated and dense line/space arrays. A higher resolution cross-sectional image of 3µm lines (Figure 5c) shows dimensions for the middle line: 3.181µm line width and 9.873µm line height (resist thickness).

5µm and 6µm lines. Larger feature sizes were also investigated. A CCL/ABF substrate with a 25µm-thick dry film resist was selected for this demonstration, resulting in lines with an aspect ratio of about 1:5. Best dose and best focus were determined using FEM. Best dose was used for the resolution demonstration. The 5µm line CDs showed less than 10% deviation from -40µm to -80µm, and a DOF of 40µm. The 6µm line CDs showed less than 10% deviation from -30µm to -100µm, and a DOF of 70m. The data from the FEMs were used to generate Bossung plots (Figure 6a). The plots show a 40µm DOF for 5µm lines and a 70µm DOF for 6µm lines. Figure 6b also includes a lower magnification image of 4.5µm, 5µm, 6µm and 7.5µm isolated and dense line/space arrays and higher resolution cross-sectional images of 5µm and 6µm lines in a 10µm-thick resist (Figure 6c).

15µm and 20µm square vias. Via resolution was also investigated (Figure 7). Best dose and best focus were determined using a FEM and a CCL/ABF substrate with 40µm-thick dry film resist; best dose was selected for this demonstration. Bossung plots were generated for both via sizes. The 15µm vias showed less than 10% deviation from -30µm to 80µm, and a DOF of 110µm. The 20µm vias showed less than 10% deviation from -40µm to 110µm, and a DOF of 150µm.

Uniformity. We used a 1.4µm-thick liquid resist film on a 510mm x 515mm glass panel and 3µm lines to test uniformity across the panel. The uniformity data in Figure 8 show a maximum CD of 3.258µm, a minimum CD of 2.988µm and an average CD of 3.099µm. Deviation ranges from -0.20% to 4.12% for an overall uniformity of 4.32%. The deviation chart shows no peaking or trending and indicates a stable exposure field.

Overlay. Overlay accuracy is essential. We used a 510mm x 515mm glass panel with a 1.4µm-thick liquid resist as the overlay test vehicle. The exposure field was 250µm x 250µm. Four shots covered the entire panel. The test procedure comprised the deposition and patterning of an initial layer, followed by deposition and patterning of a second, overlying layer. Patterning

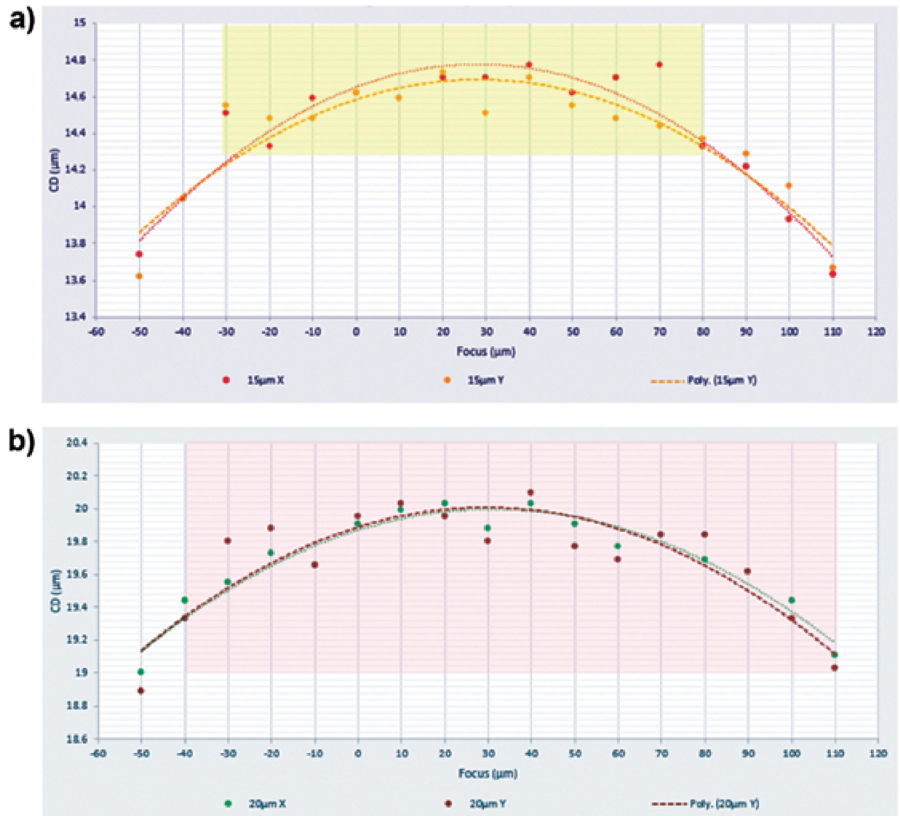


Figure 7: a) Bossung plot for 15μm vias showing 110μm DOF. b) Bossung plot for 20μm vias showing 110μm DOF.

of the second layer included site-by-site correction for each exposure field. Overlay error was checked by reading overlapped verniers (Figure 9) included at certain locations in the patterns. Each exposure field contains 3 x 3 measurement points; and 2 x 2 shots per panel were measured to determine the overlay performance. The mean +3 sigma in X was 0.91μm, and the mean +3 sigma in Y was 0.91μm. The table in Figure 9 summarizes the results of the overlay error measurements.

Summary

In this study, an extremely large exposure field size (250mm x 250mm) successfully resolved 3μm line/space features with a depth of focus >60μm on a 510mm x 515mm CCL/ABF stack with a 10μm-thick dry film resist. This study also demonstrated successful 5μm and 6μm line/space features with a 25μm-thick dry film resist and 15μm and 20μm vias with a 40μm-thick dry film resist. Fine resolution and a large field size provide the user with the opportunity to increase the package size beyond 150mm x 150mm and maintain high throughput. This new capability has the potential to pave the way

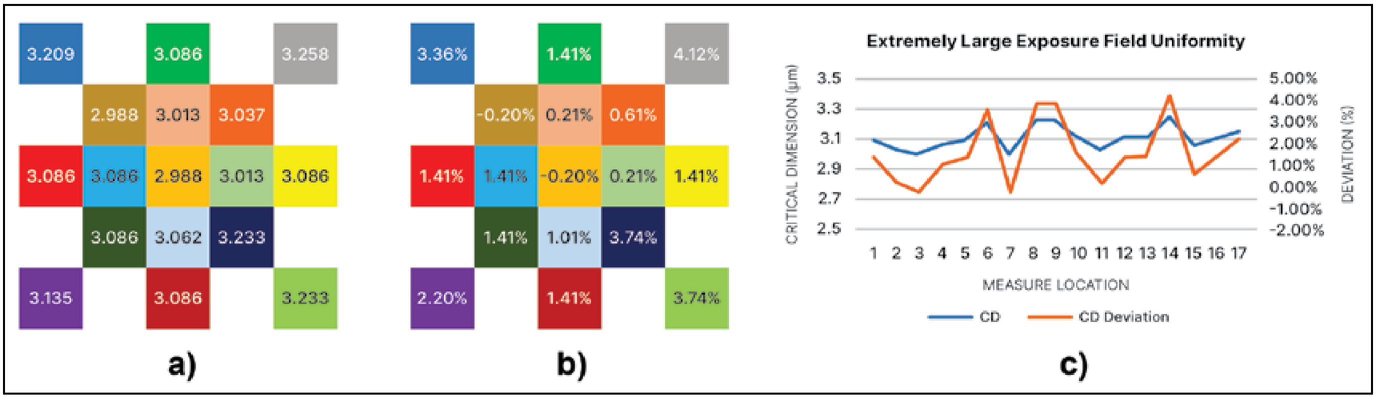
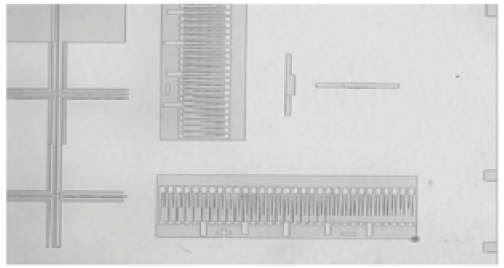


Figure 8: a) 3μm CD plot in 250mm x 250mm exposure field: The maximum CD is 3.258μm, and the minimum CD is 2.988μm; the average CD is 3.099μm, and the uniformity is 4.32%. b) 3μm CD deviation contribution map in 250mm x 250mm exposure field: The center location has a minimum deviation of -0.20% and the deviation trend up to 2.2% to 4.12% at corner locations, the maximum deviation is 4.12%, which is at the top-right corner. Overall, the deviation meets our expectation. c) 3μm CD and CD deviation chart: No trending or peak is observed. This chart indicates the CD performance with a 250mm x 250mm exposure field is stable.

a)



b)

	Dx	Dx
Max	0.52	0.39
Min	-0.32	-0.39
Mean	0.2	0.2
Std	0.24	0.24
Mean + 3σ	0.91	0.91

Figure 9: A summary of the results of overlay measurements: a) Overlapped verniers included in the pattern were used to measure overlay errors. b) The table summarizes the measured errors.

for the next generation of heterogeneous integration packages and future imaging and process studies.

Acknowledgements

The author would like to thank Timothy Chang, Casey Donaher, Perry Banks and Aries Peng for their assistance with this article. In addition, he would like to thank John Kennedy, Zhiyang Li, Karie Li and Andrew To for their work on the software algorithm, and Tom Swarbrick, Corey Shay, Ryan Tsai and Hans Lin for their support with the lithography work. The author would also like to thank all of his teammates on the X500 project for their support.

References

1. J. Chang, K. Best, J. Lu, B. Ali, M. Marshall, "Adaptive shot technology to address severe lithography challenges for advanced FOPLP," pp.: 918-923, ECTC, 2020.
2. K. Best, J. Chang, M. Marshall, J. Lu, "FOPLP lithography solutions to overcome die placement error, predict yield, increase throughput and reduce cost," International Wafer-Level Packaging Conf.(IWLPC), 2019.
3. K. Best, M. Marshall, "Advanced packaging metrology and lithography that overcomes FOWLP/FOPLP die placement error," IWLPC, 2018.
4. K. Ruhmer, "Lithography challenges for 2.5D interposer manufacturing," pp.: 523-527, ECTC 2014.
5. R. McCleary, "Panel-Level advanced packaging," ECTC 2016.
6. K. Ruhmer, P. Cochet, R. McCleary, "Panel-based fan-out packaging to reduce costs," SMTA/*Chip Scale Review* IWLPC, Nov. 11-13, 2014.
7. K. Ruhmer, P. Cochet, R. McCleary, Chen, "High-resolution patterning technology to enable panel-based advanced packaging," pp.: 129-136, IMAPS 2014, Oct. 13-16, 2014.

Biography

John Chang is a Sr. Applications Engineer at Onto Innovation, Hsinchu, Taiwan. He has a MS degree in Nanoelectronics and Photonics from National Chung Hsing U., and he has more than 19 years of experience in advanced packaging. Email: John.Chang@ontoinnovation.com.