ADVANCED PACKAGING INSPECTION SOLUTIONS FOR FAN OUT PANEL LEVEL PROCESSING

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ABSTRACT

Fan out wafer level packaging (FO-WLP) has established itself as a viable technology for high-volume manufacturing, initially, as a way to deal with shrinking die sizes, and later, in reducing package height and costs. Variations of FO-WLP, such as embedded wafer level BGA packaging (eWLB) from Infineon, integrated fan-out (InFO) from TSMC and M-Series from Deca Technologies, are now commonplace among semiconductor manufactures. The same benefits that drove FO-WLP adoption, enhanced performance, and lower costs, are now driving the adoption of fan out panel level packaging, (FO-PLP). These benefits accrue from economies inherent in the use of larger rectangular panels instead of smaller round wafers. Unlike FO-WLP, which was developed on industry standard substrate sizes (the legacy of silicon wafers), FO-PLP does not have standard substrate sizes and each competing technology presents its own unique set of challenges and benefits.

This paper discusses the process challenges and solutions that were developed to address a market that could not use existing back-end of line (BEOL) technologies the way FO-WLP did. The solutions that have evolved implement a mix of ideas drawn from the printed circuit board (PCB), flat panel and FO-WLP industries. We describe an automated optical inspection techniques meant to replace laser surface analyzers (LSA) as monitoring tools, high-resolution optical metrology using a novel illumination technique to control of copper redistribution layer (RDL) uniformity, and process control and feedback through defect inspection.

Key words: Advanced packaging, FO-PLP, RDL, Critical Dimension, Laser Surface Analyzer (LSA), Panel Level Packaging

INTRODUCTION

With the rapid growth in the advanced packaging market, specifically fan out wafer level packaing (FO-WLP), driven by smartphones and devices for the internet of things (IoT) market, outsourced semiconductor assembly and test (OSATs) suppliers have continued to pursue ways to reduce costs through improvements in yeild, materials and production processes. In a July, 2016 report, "Fan-Out: Technologies & Market Trends 2016", Yole projected growth for fan out to exceed $600 million in 2020 with "High Density" fan-out accounting for over $2.5 billion (Figure 1).

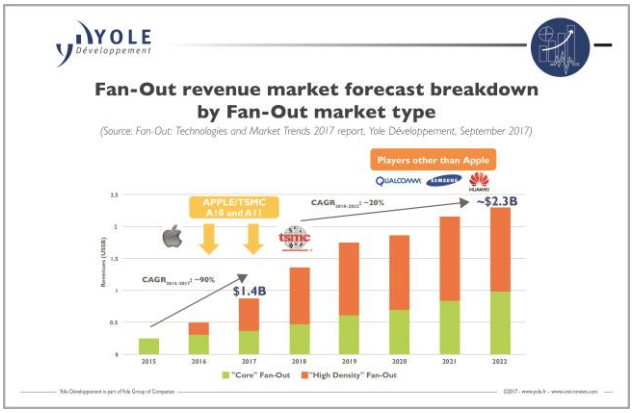

Figure 1. Fan out activity revenues by market type. SOURCE: Fan-out: Technologies & Market Trends 2017 Report, Yole Développement

Piggybacking and expanding on the development and process learning they gained during the development of key technologies in eWLB, InFO, and M-Series packaging, OSATs are now seeking further cost reductions by moving to panel based advanced packaging solutions. Simply scaling the manufacturing costs for FO-PLP in proportion to the number of packages per panel (as compared to FO-WLP) yields estimated cost reductions of 2X to 4X. A more realistic estimate, taking into account all other factors, projectscost reduction likely closer to 17% for a 10mm x 10mm package [1].

Manufacturers in an industry that has been dominated by round silicon wafers face significant challenges in transitioning to rectangular panel substrates. Companies pursuing this change have tried many different panel sizes and materials, hoping to capitalize on the economies of scale promised by the larger area available in panels. The lack of synergy in these efforts only increases the challenges and extends the amount of time it takes to address them. To further panel advancement, Fraunhofer Institute for Reliability and Microintegration has developed a consortium to address some of these challenges. [2].

A recently introduced panel inspection tool, the Firefly™ Inspection System, is an alternative to laser surface analyzers (LSA) for particle detection. It also has the ability to monitor redistribution layer (RDL) quality, which is vital to the fan out process. RDL placement, uniformity, width and spacing, as well as defect detection, must be monitored to achieve desired yields. As the industry moves to 2um Line / Space pitch, the need for monitoring and deviation detection grows while the task

becomes more difficult. In addition to process and process equipment challenges, companies are retooling their data analytics for data types that are specific to the panel process. The traceability of sub-panels and package data within a panel is crucial for failure isolation and root cause analysis .

Historically, semiconductor automated inspection methods were based on two primary illuminiations; bright field (BF) and dark field (DF) or a combination of both. This paper contrast those methods, across the areas defined, against a new illumination methodology, the patented Clearfind™ Technology, which we will refer to as method "C".

OPTICAL INSPECTION REPLACING LASER SURFACE ANALYZER

FO-WLP and FO-PLP use various wet and dry processes and process equipment. Every process tool needs maintenance, followed necessarily by tool qualification or recertification, usually including a particle test to ensure cleanliness. Unpatterened substrates are typically used to for particle detection tests. For FO-WLP, round unpatterned substrates can be scanned for particles using an LSA, which can to detect particles 80nm and smaller, and can also provide measurements of surface rougness (haze). LSAs operate by rotating the substrate at or above 1,000 revolutions per minute with low-angle illumination and wide-angle cellection of scattered light. They require a flat, uniform substrate to achieve repeatable results. Spinning a large panel substrate and maintaining flattness is a significant challenge. We have developed an alternative method that has achieved sensitivity down to 0.3µmwell suited for characterizing incoming glass substrates or monitoring physcal vapor deposition (PVD) systems that are used for copper seed layers. Figure 2 illustrates the basic principles of LSA.

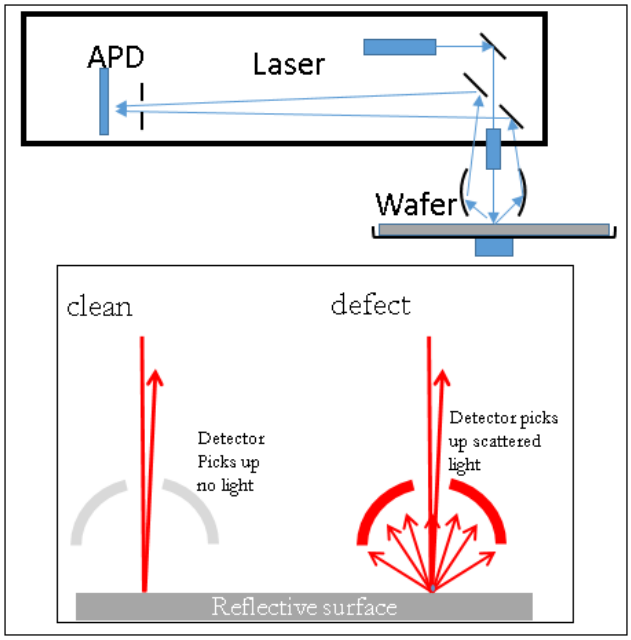

Figure 2. Simplified diagram of LSA particle detecion principles.

A similar technology was used to baseline the wafer for comparison. Figure 3 is a wafer report generated from that system on the test sample.

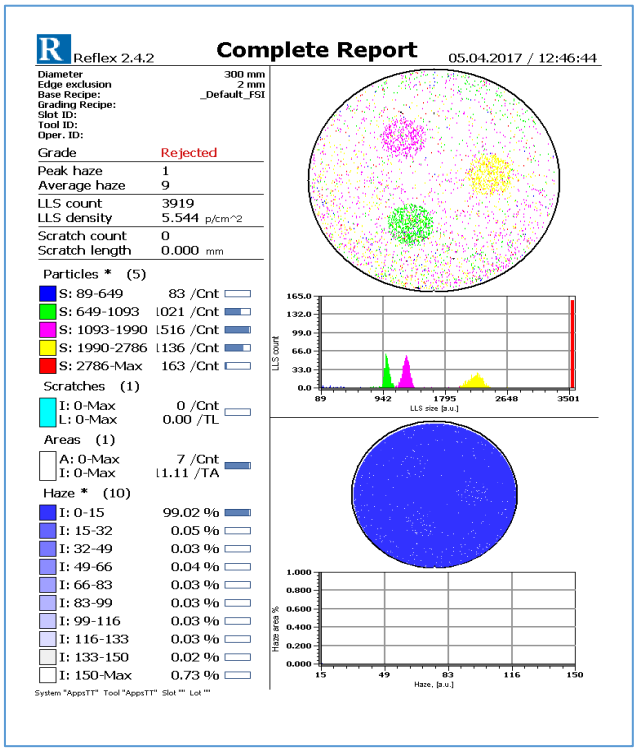

Figure 3. LSA Polystyrene Latex Sphere (PSL) reference defect map

The same wafer was then measured on our system producing the wafer map in Figure 4. An inline defect analysis and management system, was used to validate and compare capture rates. The results demonstrate equal or better performance than LSA systems currently used in production FO-WLP environments.

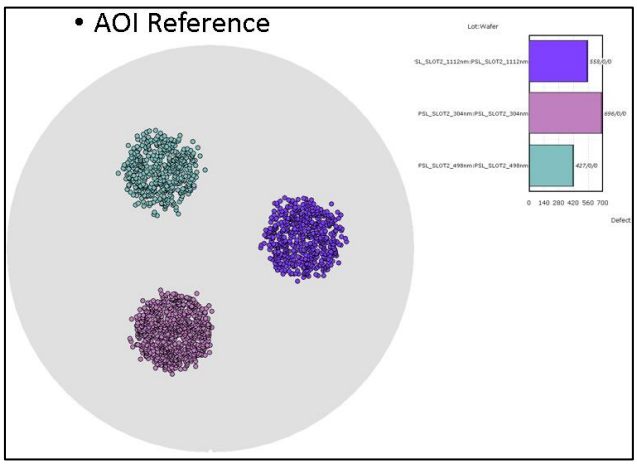

Figure 4. Inspection tool reference map used for capture rate validation against the LSA

RDL and CD PROCESS CONTROL

The inspection and monitoring of RDL for critical dimensions and line integrity is required to ensure uniform performance of the packages across the panel. Changes in dimensions will ultimately affect speed and performance [3]. In a Semi-Additive Process Flow (SAP), RDL uniformity and dimension control can be

implemented after the seed layer etch step, which defines the final Cu line aspect ratio. The accuracy of optical critical dimension (CD) measurements using bright field illumination can suffer due to surface roughness or optical distortions caused by the transparent dielectric layers within the image. As seen below, if bright field is used to measure RDL and via dimensions, the dielectric layer can obstruct the true geometry of the feature. If the optical system is under resolved, the measurements may include a repeatable added bias Figure 5 shows CD variation as measured by brightfield imaging techniques.

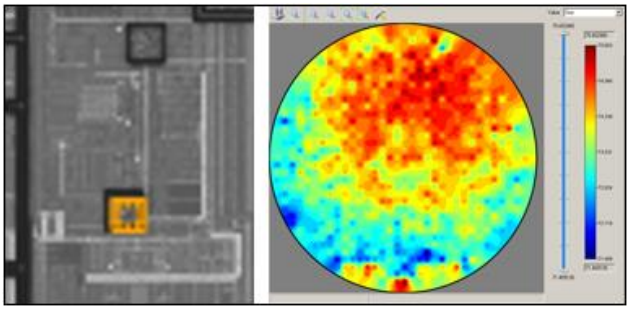

Figure 5. Whole Wafer Bright field Cu pad CD uniformity

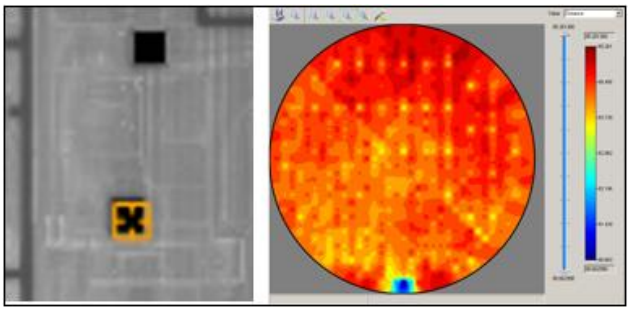

Figure 6. Whole wafer Cu pad CD uniformity using method "C"

Figure 6 shows the variation as seen using method "C" illumination. The results more accurately reflect process uniformity variations in XY dimensions are presented when measuring the "actual" open metalized area. Figures 7 and 8 show the narrow process variation measured by using method "C" illumination compared to the obstructed representation seen by bright field illumination.

Results from full wafer measurement scans are shown in Figure 7, charting the X dimension of the rectangular copper pad, and Figure 8 , charting the Y dimension of the rectangular copper pad. The brightfiled results indicate a wide radial process variation that could trigger unneeded investigation into "nuisance" excursion. The measurements provide a more accurate measurement of true process variation. Additionallly, the new illumination method can evaluate 100% of the packages on a panel with no impact on the throughput of the optical inspection phase.

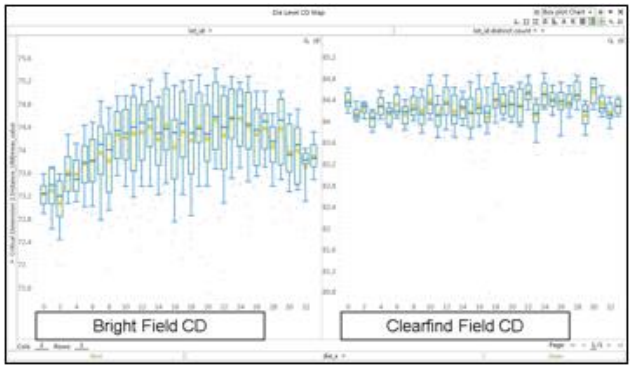

Figure 7. Cu pad X dimension CD uniformity comparing BF and Clearfind across the wafer

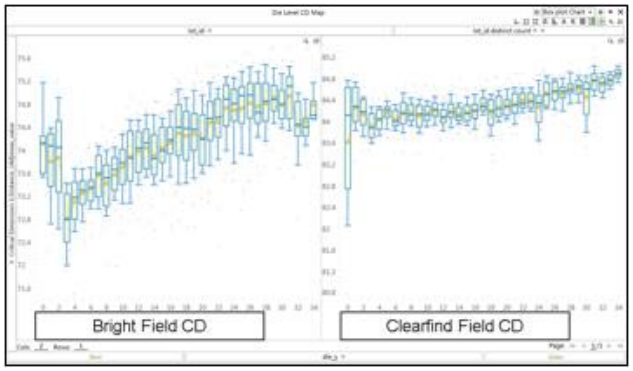

Figure 8. Cu pad Y dimension CD uniformity comparing BF and Clearfind across the wafer

The new illumination method significantly reduces image noise to allow more accurate CD measurements. Figure 9 below shows RDL images from bright field and dark field and method "C" illumination .

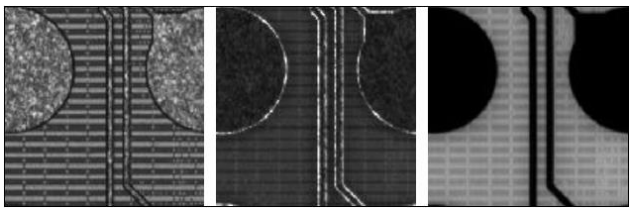

Figure 9. Bright Field, Dark Field and Clearfind CD reference images

The ability of the new method "C" technique to suppress interference from large metal grain boundries (refered to as roughness) and transparent dielectric surfaces permits accurate measurements of dimensions and reveals features that often escape detection in bright field or dark field images.

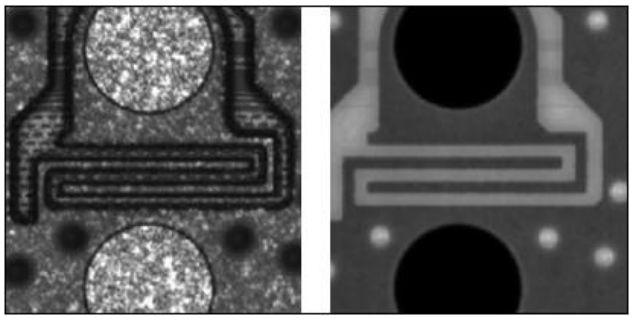

Figure 10. Bright Field and Clearfind CD reference images

Figure 10 compares bright field and method “C” images, showing the suppression of metal graininess. Graininess often causes reports of nuisance defects when random but unimportant variations in grain pattern and contrast fail to match the reference image used in the defect detction algorithm. These variations can also interfere with accurate overlay measurements, a problem that will only get worse as RDL dimensions decrease. Figure 11 compares bright field and method “C” images used for overlay measurements in a multi-layer RDL processe.

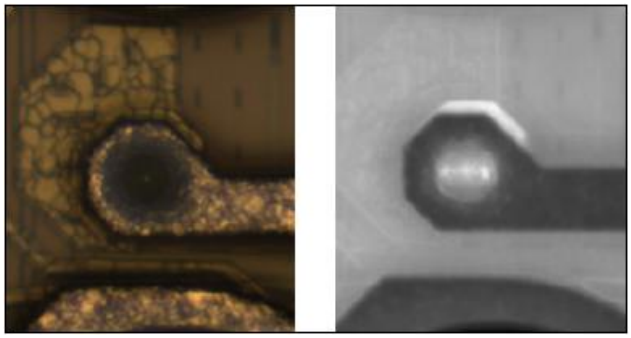

Figure 11. Bright Field and method “C” overlay reference images

Under etch causes yield losses when an incomplete etch process leaves a metal bridge that results in a short circuit.

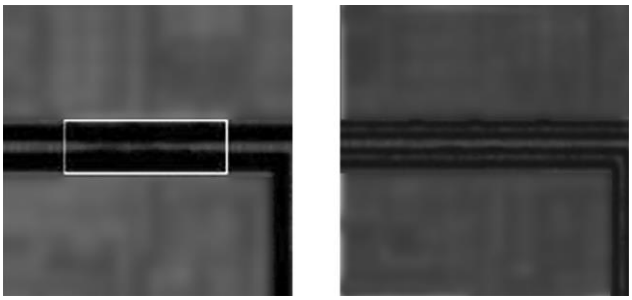

Figure 12. method “C” and Bright field Cu RDL under etching example

Figure 12 compares bright field and method “C” images of a bridging metal defect.

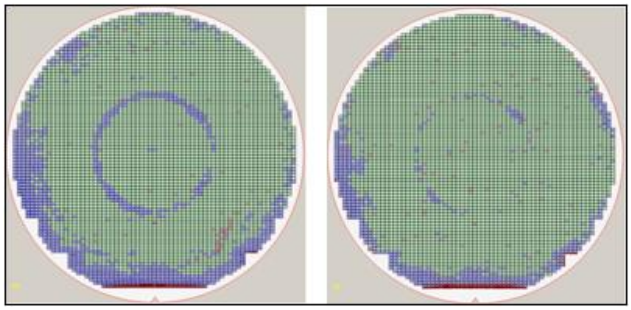

Figure 13. 2D Defect map comparing Clearfind (right) and Bright Field (left) maps of Cu RDL under etching defects

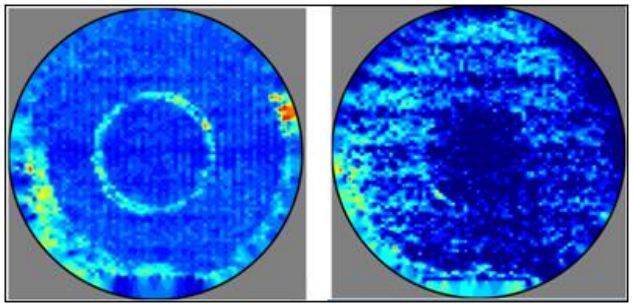

Figure 14. Whole wafer CD map comparing Clearfind (right) and Bright Field (left) Cu RDL under etching detection

In Figures 13 and Figures 14 the left images use the new illumination method. Figure 13 demonstrates bridging detection using a pattern comparison methodology where as Figure 14 utilized a CD measurement methodology to detect bridging. The defect maps as illustrated on the left hand side of Figures 13 and 14 show results from the new illumination method and clearly show greater process variation detection than the bright field illumination when performing the same inspection and metrology measurement.

PROCESS CHALLENGES IN FO-PLP

Another challenge of FO-PLP is shifting die positions causex by the EMC curing process Die and package shift can present in many forms.

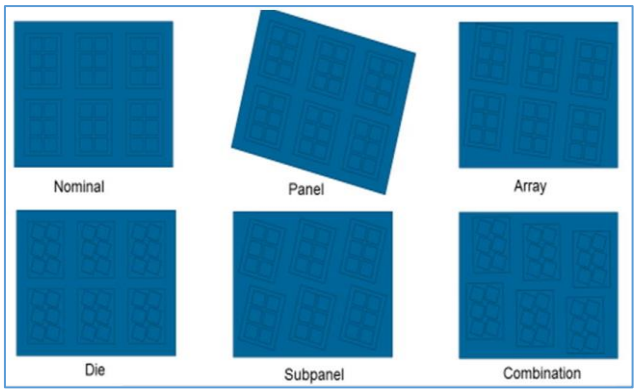

Figure 15. Panel shift scenarios

Figure 15 shows panel shift, array shift, die shift, sub-panel shift and a combination shift. Uncompensated shifts prevent accurate overlay in the RDL process. If the die/package shift is not identified and corrected during exposure, panel yield can be drastically reduced. There are advanced packaging lithography methodologies to correct the process exposure job to compensate for shift by measuring die placement and feeding corrected position infomation forward to the stepper. 2D optical metrology allows users to determine XY shift and rotation, which is then used to correct the process layer exposure. Figure 16 indicates die by die shift measurements in the X direction that would be fed forward to the stepper as overlay corrections.

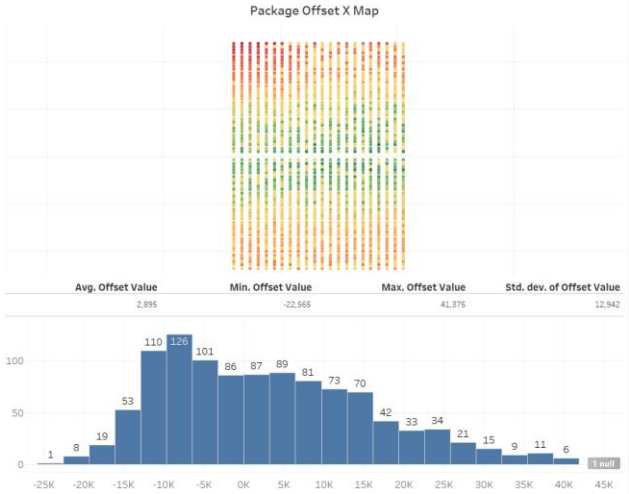

Figure 16. Package Position Shift in X as measured on a panel post EMC cure

The measurements indicate an average shift of approximately 3um . Figure 17 depicts die by die shift measurements in the Y direction, with an averae of -10µm.

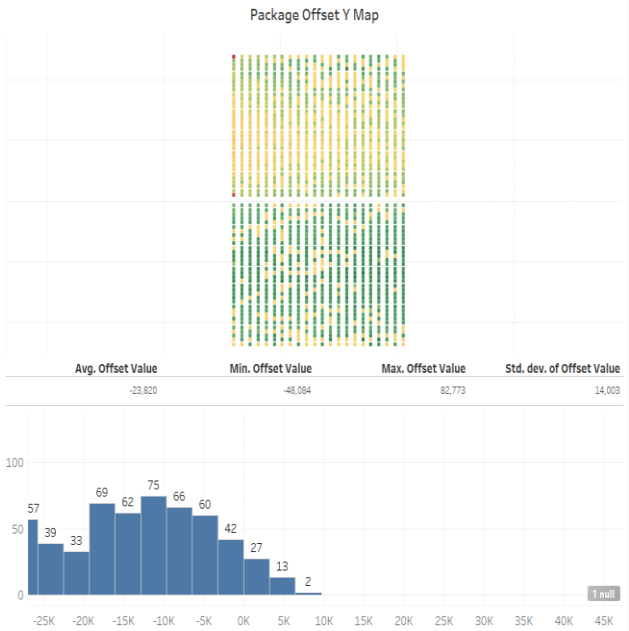

Figure 17. Package Position Shift in Y as measured on a panel post EMC cure

Managing die shift requires an exposure system stage with sufficient travel in the X, Y and Θ (rotation). Corrections to rotational shifts can be optimized by calculating and applying an overall coarse correction that reduces the residual fine correction required for each exposure. This is especially important when the stage has limited rotational capability. In the example shown in Figure 18, rotation measurements for the packages of a particular panel ranged from -9,837 to -6,077 µrads.

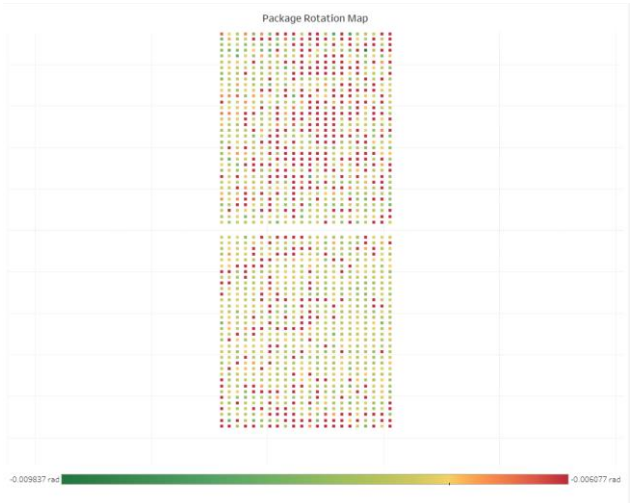

Figure 18. Package theta as measured on a panel post EMC cure

This panel also had a theta distribution as shown in Figure 19 below.

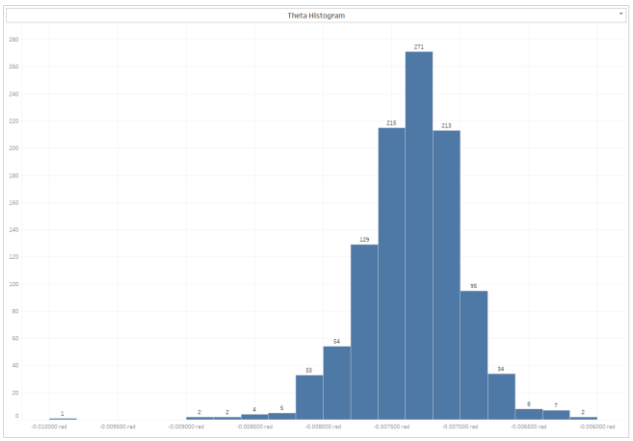

Figure 19. Distribution of package theta values as demonstrated in the panel plot of Figure 18

If the maximum correctable rotation during exposure is +/-1,000 µrad then the yield would have been effectively zero. By making a coarse rotation correction of -7,500 µrads the system could then compensate for the residual rotation during exposure, allowing approximately 94% yield.

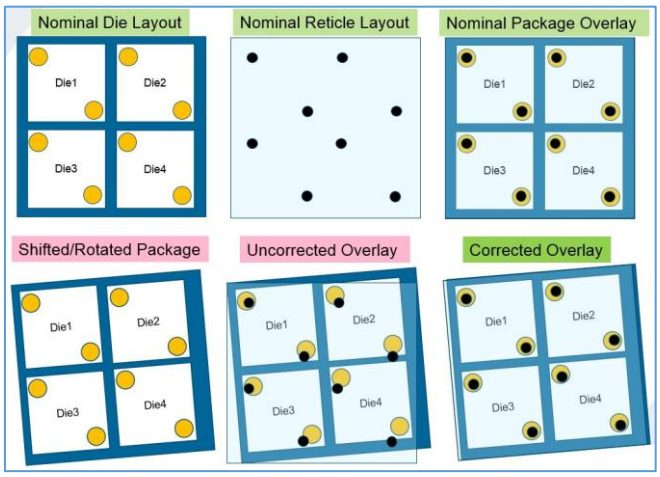

Figure 20. Overlay corrections

Figure 20 represents a 2x2 exposure package. The pick and place and mold cure operations cause shifts represented in the bottom left image labeled "Shifted/Rotated Package." Without appropriate overlay corrections, some vias would be outside the overlay tolerances as indicated in the lower middle image labeled "Uncorrected Overlay." A lithography solution enables management of the corrections to ensure proper overlay and optimal yield. Pick and place accuracy can make a significant contribution to the overall shift. Using inline inspection, metrology and coordinate measuring to monitor pick and place accuracy, a user can reduce the metrology needed in the stepper, improving stepper throughput and reducing its CoO, while at the same time reducing the number and footprint of measurement tools in the fab.

Understanding the the cured positions of packages after the pick and place operation and being able to adjust subsequent processes with predictive yield analysis will enable companies to further improve panel yields. It is imperitive to understand the data types and inputs needed to make real-time predictive yield analysis possible. Taking inputs like overlay tolerances, number of die in a package, reticle layouts and panel characteristics will enable our teams to automatically determine the best exposure methodologies by optimizing parameters such as the number of die or packages per exposure and the apporpriate overlay corrections to be applied to each exposure site.

CONCLUSION

The transition from circular substrates to rectangular panels will yield significant cost reduction benefits as long as process overhead and yield keep pace with current FO-WLP processes. We identified some of the challenges that confront the industry in this transition. We described solutions that were developed to serve a growing market segment where previously developed solutions were not applicable or were insufficient to meet the demands of the process. We also presented results that demostrate the performance of the solutions. and their efficacy in meeting the challenges. We are confident that these solutions, and others yet to be developed, will play an important role in a successful transistion to panel-based processes.

ACKNOWLEDGEMENTS

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REFERENCES

[1] C. Palesko, A Lujan, "Cost Comparison of Fan-out Wafer-Level Packaging to Fan-out Panel-Based Packaging" 2016 IMAPS Device Packaging Conference.
[2] T. Braun, M. Töpper, R. Aschenbrenner, K.D. Lang, "White Paper on Panel Level Packaging Consortium"
[3] C. Nair, H. Lu, K. Panayappan, F. Liu, V. Sundaram, R. Tummala, "Effect of Ultra-Fine Pitch RDL Process Variations on the Electrical Performance of 2.5D Glass Interposers up to 110 GHz" Electronic Components and Technology Conference (ECTC), 2016 IEEE 66th