Demonstration of Embedded Cu Trench RDL using Panel Scale Lithography and Photosensitive Dry Film Polymer Dielectrics

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Abstract

This paper presents the first demonstration of fine pitch embedded trench RDL on glass substrates using a new family of ultra-high resolution dry film photo-sensitive polymer dielectrics and a new large area panel scale lithography tool. The specific research targets are to demonstrate multilayer RDL scaling to 1um lines and vias at >200 I/Os per mm of die edge for 2.5D interposers and high density fan-out packages.

1. Introduction

High performance computing, cloud and edge networks, as well as emerging applications such as autonomous driving are fueling the demand for higher logic-memory bandwidth at lowest power consumption and cost. For the past few decades, transistor scaling resulting in more transistors per unit chip area, has been the primary approach to increasing system level performance and reducing cost. However, as chip level scaling driven by Moore's law reaches performance and cost barriers, future bandwidth increases and performance improvement need system scaling at the package level [1]. There are two ways to increase the signal bandwidth and reduce the transmission latency, (a) scale the bump pitch and increase the number of logic-memory interconnection channels, and (b) increase the data rate per channel. Integrating multiple logic and memory devices in one package, referred to as 2.5D interposers, provides a better figure of merit for signal bandwidth per unit of power and cost compared to 3D IC stacking. Compared to traditional 2D packaging, 2.5D interposers reduce the signal the interconnection length between individual devices, but more importantly, increase the number of interconnections significantly by eliminating the bottleneck of coarse pitch board-level interconnections.

Although silicon substrates made with TSVs and BEOL RDL processes were the first to be introduced in 2.5D interposer products, they are ultimately limited by the high line resistance of copper interconnects and high cost coming from 300mm wafers and low throughput unit process steps such as DRIE and CMP. Silicon based 2.5D architectures also face electrical performance challenges due to the high electrical loss of the silicon base material and high inductance TSVs. Due to the large CTE mismatch between silicon and FR-4 PWBs, silicon interposers require an additional organic ball grid array (BGA) package for board level reliability. Hence, the industry began to pursue alternate low cost interposers, primarily based on organic laminates such as by Kyocera, Shinko and Samsung, [2-4] or by embedding small silicon BEOL interconnect fabrics such as the EMIB by Intel [5]. Organic interposers, however, are limited in their RDL scaling for logic-to-memory channels by fundamental challenges such as dimensional instability and warpage driven by poor thermos-mechanical properties. Furthermore, organic packages also face chip level interconnection (CLI) reliability and chip-package interaction (CPI) challenges due to the coefficient of thermal expansion (CTE) mismatch between the chip and the package. Georgia Tech has demonstrated 2.5D glass interposers with silicon-like RDL but on large panels for potentially lower cost than silicon interposers and much higher RDL scaling capability than organic interposers [6]. This 2.5D glass interposer package, shown in Figure 1, aims to deliver an SMT mountable 2.5D interposer with high density RDL for die-to-die routing at >200 I/Os per mm. Thin glass core substrates are being used to build double-side RDL to connect test chips at 40um pitch on the top side to BGA at 500-800um pitch on the bottom side. The ultimate goal of the glass interposer R&D is to build a fully routed demonstrator test vehicle and test for board-level reliability at 40-60mm body size. A critical area of focus is on multilayer RDL materials and fabrication process tools to enable RDL scaling meeting the high I/O density needs of future high performance computing systems.

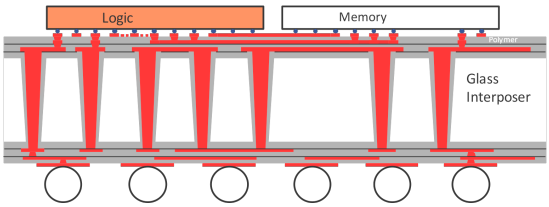


Figure 1. Cross-section Schematic of a 2.5D Glass Interposer Package with High Density RDL

Current semi-additive processes used for RDL on wafer and panel scale are limited to routing densities less than 100 I/Os per mm. GT PRC has proposed and already demonstrated a new paradigm in multilayer panel scale RDL using Via in Trench (ViT) and Via in Line (ViL) structures at 2um lines and 2.5um vias for silicon like RDL on large glass panels for the first time [7]. The exceptional dimensional stability of glass in thicknesses down to 30um, enables via capture pads to be almost the same size as the vias, resulting in "padless" interconnections between layers. This paper focuses on lithography processes to achieve photo embedded trenches of 2-5um critical dimensions with a high-resolution photo-sensitive dry film dielectric from TOK Japan, and a large area

projection stepper lithography tool from Rudolph Technologies, Wilmington, MA. A major limitation of BEOL interconnects is the high line resistance caused by the small cross-section of the copper traces. The approach presented in this paper is targeted at high aspect ratio copper traces with 2um widths and 5um copper thickness, to achieve close to silicon BEOL routing density but at much lower line resistance than BEOL interconnects, enabled by the photo-dielectric material and lithography tool.

2. Embedded Trench RDL Process

A comparison of semi-additive process (SAP) used in current package RDL fabrication, and embedded trench copper process used in this paper is shown in Figure 2.

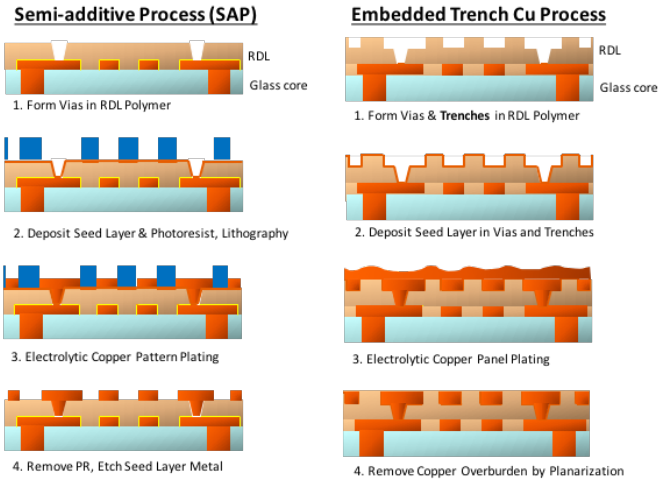


Figure 2. Comparison of Process Flows for SAP and Embedded Trench RDL Fabrication

Traditional semi-additive process (SAP) methods to form RDL wiring have been limited in scaling to 5 µm wiring [8-10], and face several challenges in scaling below 5 µm. The process limits are the side etching of the copper lines during seed layer removal and poor adhesion of ultra-fine copper conductor lines on smooth polymer dielectric surfaces. This research explores new photo-sensitive ultra-thin polymer dry film dielectrics and panel scale lithographic tools to form trenches and vias, and also demonstrates a new integration method to address the scaling challenges of SAP by eliminating side etching of the copper lines. The reduction of the via capture pad size is an important requirement to achieve the target wiring density, and is enabled by improving the positional accuracy of the micro-via formation process and by selection of dimensionally stable core materials. The use of photo-sensitive materials and lithography to form both vias and trenches enables high precision layer to layer registration by eliminating the location tolerances associated with serial laser via formation processes. As a core material for this research, glass was selected because of its superior dimensional stability compared to organic laminate composites, low electrical loss and large panel availability [11,12].

3. New Photo-sensitive Dry Film Polymer Dielectric

This paper introduces a high resolution, photo-sensitive dry film polymer dielectric material in ultra-thin film thicknesses down to 10µm and 5µm. Although liquid photo-sensitive materials such as photo-sensitive polyimide (PSPI) have been widely used in RDL fabrication on silicon and fan-out wafers, the new IF series dielectric from TOK Japan achieves a compelling combination of large panel lamination compatible ultra-thin dry films, high lithographic resolution down to 2µm, and low cure temperature below 200ºC.

Material Properties of IF film: Electrical and thermo-mechanical properties are critical for RDL dielectric materials, in addition to their photo lithographic capability, for both SAP and embedded trench process integration. The IF dry film was designed to meet those requirements as an ideal dielectric material candidate. The main structure of the IF film is epoxy polymer, which is widely used as a dielectric in conventional package manufacturing today and has proven long-term reliability. In addition to its excellent reliability, IF dry film has excellent lithographic resolution with both i-line and ghi-broad band lithography tools. This paper demonstrates 2um line and space resolution with 5 um film thickness on silicon and glass substrates.

Thermal and Mechanical Properties: Several material properties of IF dry film were measured and are summarized in Table 1. The glass transition point (Tg) was 250^{0}C and thermal decomposition temperature detected by TG/DGA showed stability up to 300^{0}C, indicating the endurance of IF films during solder reflow processes (260^{0}C). On the other hand, IF films can be cured under relatively lower curing temperatures with short time (200^{0}C for 1 hour) after the photo lithography process, a major benefit of using an epoxy polymer. Regarding the mechanical properties, the IF dielectric film with its low modulus (1.6 GPa) and high elongation to failure (20 %) has excellent stress absorption characteristics for long term reliability and reduced substrate warpage. It also has an appropriate CTE (45×10^{-6}/°C) for multi-layer RDL stress control.

Table 1. Key Properties of IF Photo-Sensitive Dry Film

Properties	**Measurement method**	**IF4610**
T_g (°C)	DMA	250
CTE (x10^{-6}/°C)	TMA	45
Thermal weight loss temperature (°C)	TG/DTA	315 (3%)
		325 (5%)
Elongation to break (%)	Tensilon	20
Tensile strength (MPa)		82
Young's modulus (GPa)		1.6
Dielectric constant	CV, 1MHz	3.5
Loss Tangent	0.1 MHz	0.022

Adhesion strength: Adhesion strength with sputtered Ti/Cu was characterized by a standard peel test method, before and after unbiased HAST (Highly Accelerated Stress Test). Pre-

conditioning for the peel test structures was conducted according to Moisture Sensitivity Level 3 (MSL-3) following JEDEC standards. The MSL-3 test included a prebake step at 125 ^{0}C for 24 hours to remove all the moisture in the samples, followed by moisture soaking in a humidity chamber at 60^{0}C, 60%RH for 40 hours, and finally three cycles of solder reflow process with a peak temperature of 260^{0}C. A schematic of the peel test structure is shown in Figure 3. The IF film exhibited good peel strength, with no significant change before and after the HAST testing (0.7kgf/cm)

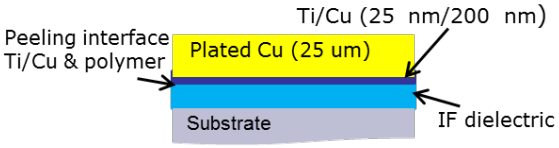


Figure 3. Cross-section Schematic of the Peel Strength Test Structure

4. Panel Scale Lithography Tool

Most front-end tools have high numerical aperture (NA) lenses with low depth of focus (DOF) that prevent adequate penetration of thick films with sufficient image contrast to achieve the side wall angle and resolution requirements. Although photoresist sidewall angles are primarily a function of the photoresist material and its processing (pre-bake, post-bake, developing, etc.), the exposure system plays an important role. Accurate focus control across a substrate is required to achieve consistent and accurate CD control with straight and perpendicular side walls.

The lithography stepper employed in this study was a Rudolph Technologies JetStep® G45 HR System with a UVLED i-line illumination source, shown in Figure 4. The system utilizes "on the fly" focus control to ensure that every exposure is at the optimum focal plane. This capability is essential when advanced packaging substrates become warped by film stress and thermal cycling. The system's 200mm lens field and 0.15 NA provide a resolution of 1.5um with a large DOF to maintain image integrity and CD control.

Figure 4. Jetstep® G45 Panel Scale Lithography System

5. Panel Scale Lithography Results

Photo lithography of the IF dry film is based on epoxy polymerization, initiated by photo acidic initiators. The reaction is then accelerated by a PEB (Post Exposure Bake) process. After the PEB, un-polymerized areas are removed by immersion development with PGMEA (Propylene glycol mono methyl ether acetate) solvent. Finally, the film is fully cured to complete the polymerization reaction. The photolithography process for patterning of small vias in IF4605 material is summarized in Figure 5. These steps include:

(A) Vacuum lamination of IF4605 film on a substrate

(B) UV exposure (365 nm i-line or ghi-broad band) and post exposure bake process (90°C for 5 min)

(C) Development by PGMEA and then thermal curing (200 °C for 1hr)

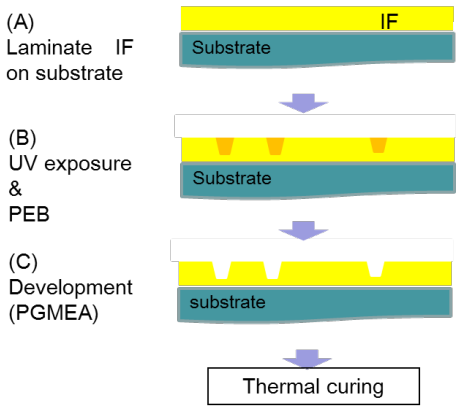
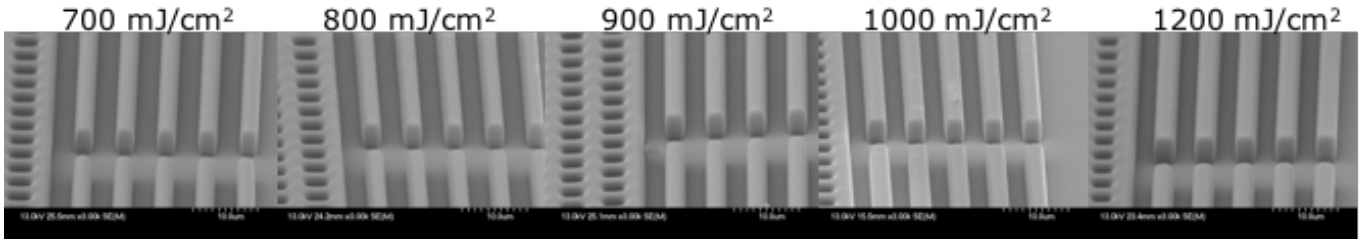
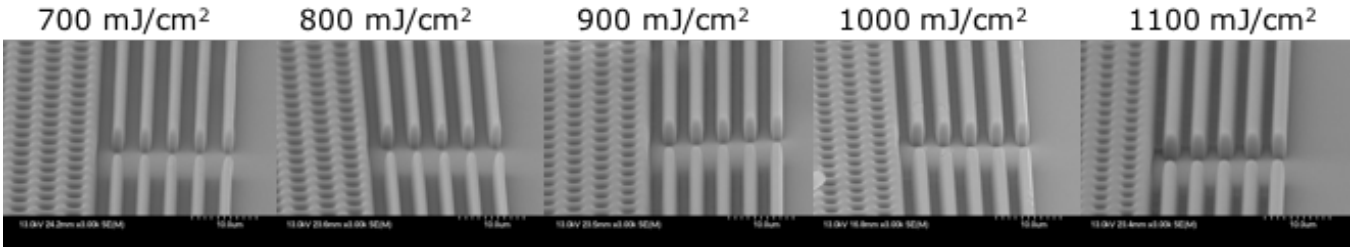


Figure 5. Lithography DoE Process Steps for IF4605 film

A series of design of experiments (DoE) were conducted to establish the process windows for the IF 4600 series films using the Rudolph Jetstep® G45 HR lithography tool. For these tests, 8 inch Si wafers were used as the substrate, and IF4605 (5 µm thickness) was vacuum laminated using a Meiki MVLP-300 tool at Georgia Tech, at 0.9MPa for 30 seconds. The exposure was done using the G45 HR system from Rudolph Technologies, followed by PEB and development at the demonstration labs at Rudolph Technologies. After this step, the samples were sent back to Georgia Tech for final rinse cleaning and oven drying. The test structures in the design had a CD range of 1.5 to 15µm, and the samples were inspected by optical micrography as well as scanning electron microscopy (SEM). Only the SEM results and analysis are presented here. The exposure dose was varied from 300 to 1200 mJ/cm^2 in increments of 100mJ/cm^2, and the focal position was varied from -12µm to +12µm in 3µm increments. Figure 6 illustrates the SEM micrographs from the lithography DoE for a range of exposure doses. As seen in Figure 6a, excellent line definition was observed with a dose range of 700-1200 mJ/cm^2 for a 3µm CD, with 900-1000 mJ/cm^2 dose providing the best CD control. For the 2µm CD SEM micrographs shown in Figure 6b, similar results were observed, but with a slightly narrower process window.



(a) 3μm CD



(b) 2μm CD

Figure 6. (a) Exposure Dose Range of 700-1200 mJ/cm^2 for CD of 3μm, and (b) Exposure Dose Range of 800-1100 mJ/cm^2 for CD of 2μm, both indicating good lithographic definition and CD control

The results from the depth of focus study for 2μm, 3μm and 5μm CDs are shown in Figure 7.

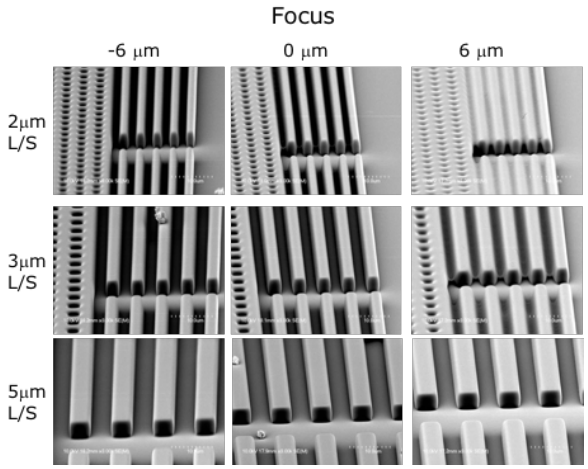


Figure 7. SEM micrographs of IF4605 lithography with variation in the focal depth.

As seen in the figure, the large depth of focus capability of the Jetstep® tool enabled excellent resolution over a wide range of focal depths, with 5μm features defined well from -6μm to +6μm, and 2μm lines and spaces defined well from -6μm to +3μm. There is some bridging of features seen at a focal depth of +6μm for the 2μm features. These results indicate that the control of warpage in the panel is still a critical factor in achieving ultra-fine trench widths for the embedded copper trace process.

6. Photo-Embedded Trench Process Demonstration

After optimizing the lithography process to form ultra-small trenches in IF4605 films, Ti-Cu seed layers were deposited by PVD, followed by electrolytic copper plating to fill the trenches. This process resulted in few microns of copper overburden on the surface of the dielectric. This additional copper was removed by using a novel fly-cut planarization process developed by Disco Corporation, Tokyo, Japan. Further details of this process and tool are described in previous published work [13]. A successful demonstration of ultra-fine embedded copper traces down to 2μm in IF4605 dielectric on glass core is shown in Figure 8.

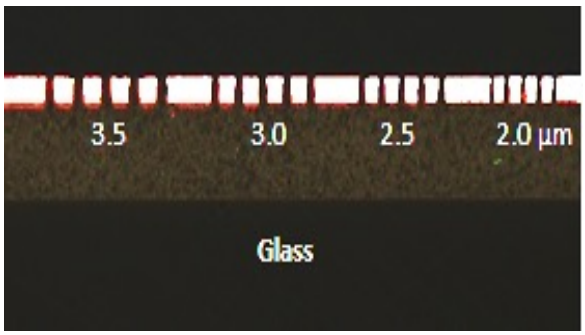


Figure 8. Cross-section micrograph of 2μm to 3.5μm embedded copper traces formed in IF4605 dielectric

The panel scale fly-cut planarization process also results in an ultra-smooth surface with average surface roughness (Ra) in the range of 20-30nm as shown in Figure 9. Such a smooth surface is ideally suited for multilayer RDL fabrication at ultra-fine pitch.

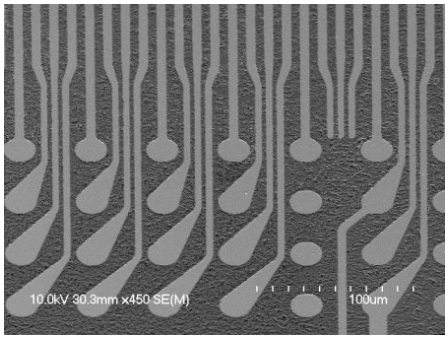


Figure 9. Top View of 3.5µm line width and 2.5µm space embedded copper structures at 40µm I/O pitch

7. Conclusions

This paper demonstrated ultra-fine line and space RDL down to 2µm on glass interposers, enabled by the combination of a new ultra-thin 5µm dry film photo-sensitive epoxy dielectric material, namely IF 4605, and a high resolution large panel scale lithography tool, JetStep®. A series of design of experiments (DoE) were conducted using 200-300mm wafers as a starting point to characterize the lithographic performance of the TOK IF series dry films in 5 and 10um thicknesses using the Rudolph Jetstep® tool platform. The key process parameters such as the depth of focus and exposure dose were evaluated, and wide process windows for both the exposure dose and depth of focus were achieved. We successfully demonstrated 2µm lines and spaces embedded trenches with excellent side wall quality and near vertical profiles. The high depth of focus window observed during the experiments will allow for a small amount of warpage at panel scale.

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