Optimizing advanced IC substrates (AICS) for PLP

By Keith Best [Onto Innovation]

Faster data transfer, greater heat dissipation, less power consumption and increased functionality are all qualities that chipmakers and their customers want from their devices. Since the dawn of the semiconductor industry, the pursuit of increasingly advanced nodes has served as the industry's North Star. But for today's voyagers, rough seas are ahead: these nodes have decreased in size, input/output (I/O) bumps on the chip have grown smaller—and with the shrinking of these bumps, their ability to mate directly to printed circuit boards (PCB) diminishes. The way to avoid this is to use advanced IC substrate (AICS), i.e., an intermediary substrate that enables progress in panel-level packaging (PLP) and chiplets.

Chiplets are a type of advanced packaging in which multiple die—such as memory, analog and other devices—are assembled in a single, large package along with a central processing unit (CPU) or graphics processing unit (GPU). With AICS, all of these chiplets can be co-packaged together in packages that may be as large as 120mm x 120mm each, which is a considerable increase from the 10mm x 10mm-sized packages of fan-out panel-level packaging (FOPLP). These large packages allow multiple die with smaller interconnects to be assembled and then redirected to larger contact bumps compatible with a PCB. None of this means the industry has left the pursuit of next-generation advanced nodes behind, or smaller packages for that matter.

Although the semiconductor industry has turned to chiplets and other advances to meet various next-level performance needs and spur new innovations, advanced nodes remain key areas of development and advancement. But this move toward extra-large AICS packages signals the need for large exposure field, fine-resolution panel-level lithography systems that can expose entire panels using fewer exposures. The journey to a new era of chiplets and PLP, however, is fraught with challenges that must be overcome, including total overlay shift, yield loss and copper-clad laminate (CCL) substrate distortion. In this article, we will focus on these three challenges to the rapidly growing AICS market and outline several solutions that we have determined will enable manufacturers to address them.

Total overlay drift

The AICS substrate that enables PLP and the segments it serves (e.g., the emerging industry star artificial intelligence [AI]) features up to 24 redistribution layers (RDL) split between the frontside and backside of the substrate. While having such a large number of RDLs improves the package's I/O count and functionality, these improvements are not without their complications. For example, as the number of RDL layers increases, minimizing overlay errors becomes increasingly burdensome. Furthermore, the trouble with overlay errors is not merely a layer-to-layer issue. Total overlay drift—the compounded drift of all RDLs in an AICS—is a challenge that advanced packaging manufacturers will need to address. But first we need to discuss how RDL processing affects the substrate.

During the AICS process flow, the buildup film between the RDLs is cured after each laser-drilled via layer. This continuous thermal cycling of the CCL substrate has the potential to distort the substrate in each quadrant of the panel. The result is that each quadrant could have vastly different overlay results.

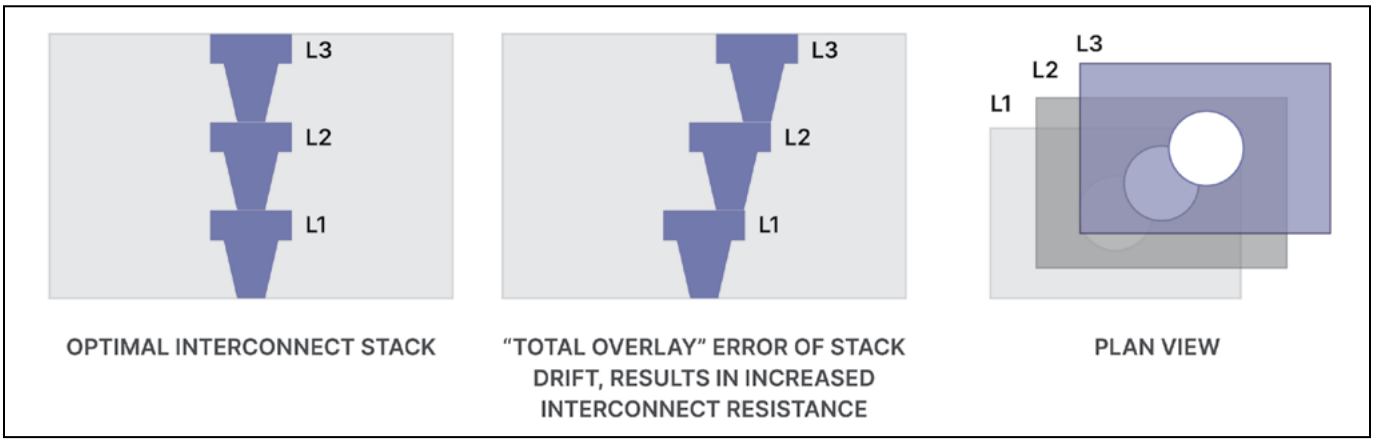


Figure 1: A visual explanation of total overlay drift.

And in the case of extremely large exposure field (e.g., 250mm x 250mm) lithography systems, these differences in overlay create a major yield challenge, especially for high-volume manufacturing.

First, let's define total overlay. Total overlay is the summation of the overlay errors for all RDL layers, with respect to the bookending final layers on either side of the panel (**Figure 1**). Cumulative overlay drift from individual RDL buildup layers can significantly increase overall trace length. This may result in higher interconnect resistance, parasitic effects and poor performance for high-speed and high-frequency applications.

As each RDL is added to the film stack, layer-to-layer overlay data needs to be continuously monitored. If the total overlay error exceeds specifications at any point, and at any location on the panel, corrective action must be taken to mitigate total overlay drift or else the design resistance specifications for a package may be exceeded.

You can think about total overlay like this: if the overlay drifts 5µm per layer, and there are 10 layers, the total RDL length will increase by 45µm. This problem is exacerbated as the number of layers increases, i.e., in a 24-layer RDL stack, the interconnect length would increase by 115µm.

To address the total overlay challenge, manufacturers should employ an overlay tracking system, one that incorporates metrology, lithography and analytics that records measurements for every RDL-to-via overlay across the entire panel and sums the vectors, from layer to layer, as the process stack grows. With such a system, the manufacturing team could use inspection and data analytics to track and compensate for multi-layer overlay drift. The tracking system would generate an error signal when cumulative overlay error exceeds thresholds, and the required overlay correction offsets would then be calculated and sent to the lithography system. Without a suitable tracking system in place, manufacturers have no way of knowing if RDL resistance meets specification until final electrical test (e-test). By that point, resources, time and money will have been wasted.

Yield challenges

Now that we've discussed total overlay drift, let's explore AICS package yield and its importance in fostering a cost-effective, high-throughput process. As previously mentioned, AICS have relatively few packages per panel. For example, a 510mm x 515mm AICS panel can only accommodate 16 packages (120mm x 120mm) compared to FOPLP, which could have over 2,300 packages. That's a significant difference. One defective package on an AICS could result in a 6.25% yield loss, whereas with FOPLP, one defective package may only represent a 0.04% yield loss.

To make matters even more complicated, the yield challenge is exacerbated because as the AICS package size increases to 150mm x 150mm, a single defective package failure results in an 11% yield loss, which is a significant decrease in an industry that operates under extremely narrow margins. In addition, the requirement to process both the frontside and backside of the AICS offers another risk: surface contamination leading to defects that result in yield loss.

It takes a few weeks to complete the processing of an AICS. Only by knowing the yield of an entire fab's AICS inventory, in real time, will productivity be evaluated accurately. Furthermore, panel yield needs to be assessed in terms of

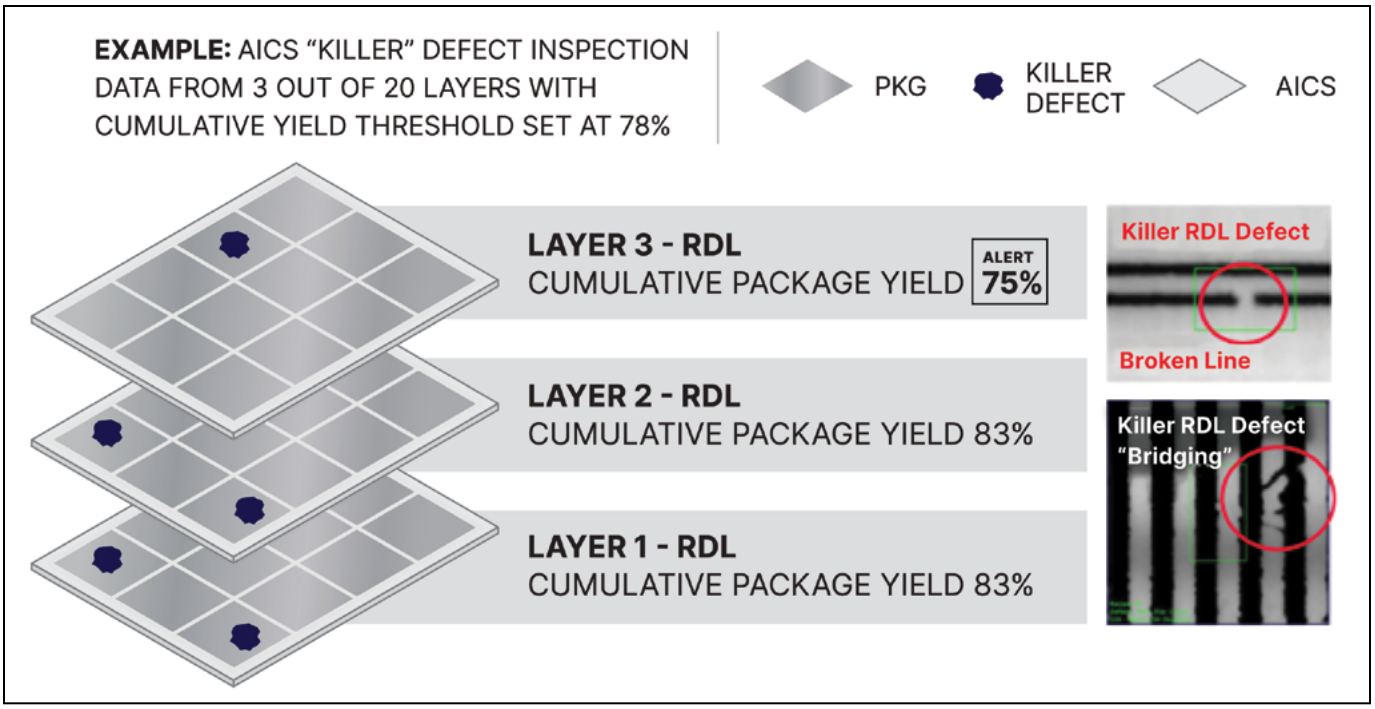


Figure 2: The effect of defects on cumulative package yield.

cost at each process step. The AICS process is a die-last process, so the panel is not of high value until the die are placed at the very end of the build. Knowing when to scrap, restart or continue to process low-yielding AICS becomes a business decision, one that relies heavily on accurate yield data. Of course, the yield loss needs to be investigated and root causes identified as soon as defects, both potential and actual, arise. With this in mind, if the manufacturing team learns that the panel at layer five in the process has a yield of 50% and it's a 40-layer process, is it worth processing the panel further? Should the panel be scrapped and restarted? The likely answer is, yes (**Figure 2**).

This is where the use of advanced automatic defect classification (ADC) and yield analytics are imperative for a quick and successful recovery. To track the panel yield, a comprehensive and intelligent yield-tracking database, with access to inspection data for each panel at each process step, is needed. In addition, the inspection data requires an ADC system trained to identify killer defects. These killer defects—such as RDL opens, RDL shorts, missing vias and via residue—must be classified with 100% accuracy, so that each defective package on the panel can be identified with confidence. However, some defects may not be apparent until later in the process. For instance, a large particle embedded in the build-up film may not impact the current via layer, but a later RDL pattern that is located on top of the particle could induce RDL bridging due to the particle creating an out-of-focus lithography condition.

As the industry transitions to glass core substrates that may allow for single-side processing, future AICS processes may become more robust. However, package sizes will continue to grow, and RDLs will continue to shrink below a line/space of 5µm. This is a problem for the build-up film because it is not capable of supporting laser-drilled vias less than 10µm. In other words, the technology roadmap will require new photoresist and photo-imageable dielectric processes.

Copper-clad laminate distortion

Now that total overlay and yield loss in AICS have been discussed, let's move on to a discussion about how CCL processing leads to panel distortion and how overlay correction solutions compensate for this. To start with, let's talk about the curing of buildup film. CCL substrate processing requires the curing of buildup film. During this process, the CCL substrate is subjected to repeated thermal cycling, resulting in the distortion of the X and Y coordinates of the interconnect patterns. This distortion impacts the registration of the laser-drilled vias to the lithography-printed RDL.

Here's where the CCL process gets challenging: RDL design typically includes a large landing pad at the end of each interconnecting line/space (l/s) that connects to the vias. The landing pad is significantly larger than the critical dimension of the RDL. By including this feature, the overlay tolerance is increased significantly. For example, if the diameter of the laser-drilled via hole is 30µm, the RDL landing pad could be 50µm to provide an overlay tolerance of +/-10µm. With the interconnect technology roadmap approaching a point of inflection—from 12µm/9µm l/s to below 5µm/5µm l/s—it becomes increasingly difficult for advanced packaging designers to meet this challenge because the large landing pads limit design space. This results in the need to increase the number of RDL layers, along with an increase in cost and potential yield loss. To mitigate this design quandary, smaller RDL landing pads are required, but this can only be achieved if process overlay is improved. With improved overlay performance, RDL and via structures with smaller landing pads can be squeezed into a smaller area, eliminating the need for additional RDL layers. Moreover, this reduces the cost and yield loss risk—i.e., fewer layers mean fewer worries.

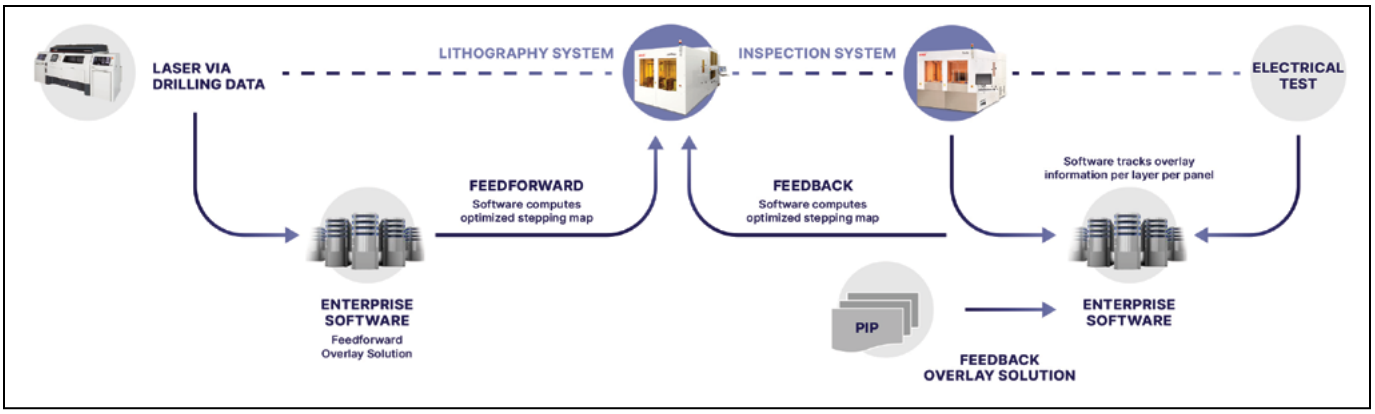


Figure 3: Overlay solution for AICS panels.

To improve process overlay, the lithography system, or stepper, must analyze and compensate for CCL substrate distortion errors. While this sounds simple in principle, the CCL distortion components are complex and extend beyond the traditional six-parameter model supported by most lithography steppers. This nonlinear distortion requires additional higher order lithography system corrections, thereby increasing the complexity of the model.

The stepper's ability to correct for the substrate distortion is only part of the solution. We also need accurate metrology data to generate optimum alignment solutions to compensate for distortion errors. Typically, this data is only available after the lithography process is finished and overlay of the vias to the RDL landing pad is measured. The data is then analyzed and sent back to the stepper to correct panel distortion for future incoming panels (a.k.a. feedback corrections). However, the feedback corrections are only relevant if the panel distortion remains constant for incoming future panels. Sampling plans and periodic metrology can help generate a run-to-run solution. These steps, together with artificial intelligence (AI) and machine-learning software, can correct the dynamic distortion errors exhibited by CCL substrates over time.

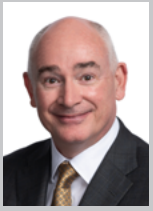
An alternative approach could be to gather metrology data from the substrates after the laser-drilled vias have been created and before the stepper is involved. These are known as feedforward corrections. Feedforward metrology requires a leap of faith, however, because it depends on a laser-drilling tool and stepper working in concert to produce an accurate and reliable dataset to create the stepper alignment solution (**Figure 3**).

In principle, the ideal solution to solve the overlay problem would be to use a feedforward approach where X and Y coordinate data from the laser-drilled via holes are employed to generate an alignment solution. The overlay metrology data will confirm if the feedforward correction is accurate and will highlight the residual errors. If the residual errors are significant, the feedforward model likely needs to be adjusted. Ironically, post-exposure, final overlay metrology could be used to optimize the feedforward model. With machine learning and continued iterations, the model could be continuously adjusted to achieve good overlay with low residuals.

The manufacturing of large packages requiring the heterogeneous integration of chiplets, high-bandwidth memory (HBM) and GPU/CPU is only achievable using AICS processing. To deliver this capability, substrate distortion needs to be characterized and compensation provided in order to maintain high yields and reduce costs. A comprehensive metrology and lithography solution is required. This solution should be used in conjunction with advanced software that can automatically adjust models to compensate for the dynamic substrate distortion components. This approach could extend the roadmap of CCL substrate manufacturing beyond its current design limits, thereby reducing costs and improving yields.

Summary

With the AICS market forecast to reach nearly $25 billion in 2027, according to Yole Group, there is little doubt that AICS will be one of the chief drivers of innovation. However, AICS brings with it significant challenges, like total overlay shifts, yield loss and CCL substrate distortion. And with the number of RDLs soaring to 24 with AICS, any unaddressed errors in any single layer can ruin a substrate that otherwise would have been used in a PLP. However, by applying the techniques in this article, manufacturing teams can improve yield and throughput and reduce costs in this emerging PLP segment of the semiconductor industry, guiding manufacturers away from turbulent waters and steering their ships toward smoother seas.



Biography

Keith Best is the Director of Product Marketing, Lithography, at Onto Innovation, Wilmington, MA. For more than 35 years he has held a range of semiconductor processing and applications positions for both device manufacturing and capital equipment companies. He also has numerous publications and holds 22 US patents in the areas of photolithography and process integration. Email keith.Best@ontoinnovation.com