Measuring the Critical W-recess in 3D NAND

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A new technique that uses a specialized via to periphery target structure overcomes limitations of existing approaches.

LAST SUMMER, THE SEMICONDUCTOR industry reached a significant milestone: one of the world's top-tier fabs had begun production of the first 3D NAND chip with more than 200 layers. The announcement was significant but not a shock. Several other fabs had been progressing toward breaking the 200-layer barrier, so reaching the milestone was not a matter of if but when.

As significant as this advance is, the high-volume manufacturing challenges of producing high-aspect ratio (HAR) 3D NAND chips are considerable. One challenge is the ability to measure the tungsten (W) recess to the bottom of a 3D NAND device following the replacement gate process. Presently, there is no in-line process control solution that can accomplish this. The reason for this is known: beyond just a few layers in the stack, the W recess becomes opaque in the ultraviolet/visible/near-infrared region, the realm of many OCD systems, after just a few layers in the HAR stack. Additionally, increased wordline slit pitch scaling further reduces the already minimal optical signal from the top of the 3D NAND structure to the bottom.

Both of these matters present a challenge for manufacturers because the ability to measure the W recess is critical. Under-etching the W gates in the recess will cause wordlines to short, while over-etching the W gates could damage cells adjacent to the wordline slit or cause a short from the wordline to the source line.

Fortunately, a new technique can overcome these W recess challenges in HAR 3D NAND devices.

By using finite-difference time-domain (FDTD) and optical critical dimension (OCD) simulations, we were able to determine that a specially designed, design rule-compliant ellipsometry target enables mid-infrared (IR) light to penetrate through metal oxide pairs to reach the bottom of the W recess, thus enabling the measurement of the Z-profile of the W recess. Equally as important for the future of HAR devices, this data demonstrates that mid-IR light can overcome the challenge of reaching the bottom of a W recess in a 3D NAND chip with more than 200 layers, a step that might be significant in the proliferation of these devices.

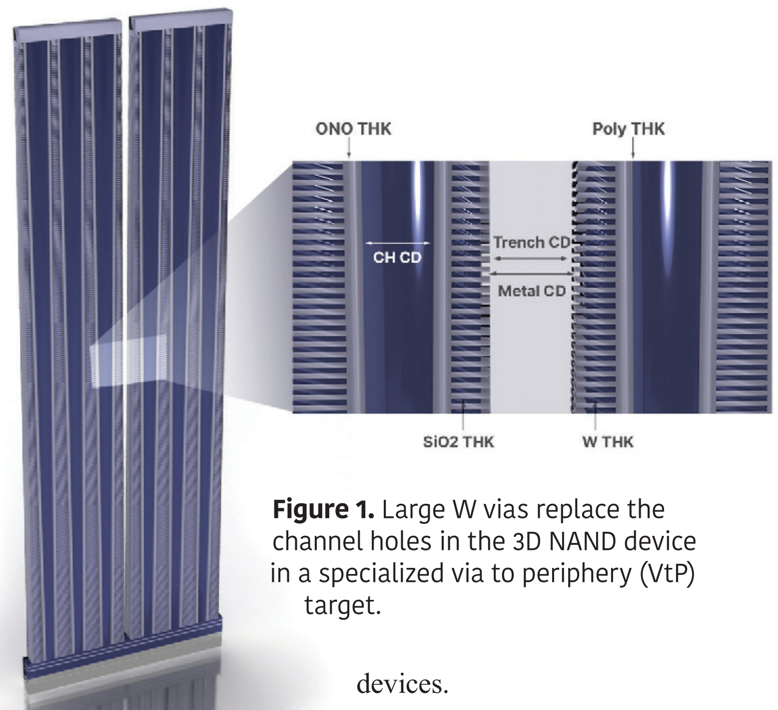


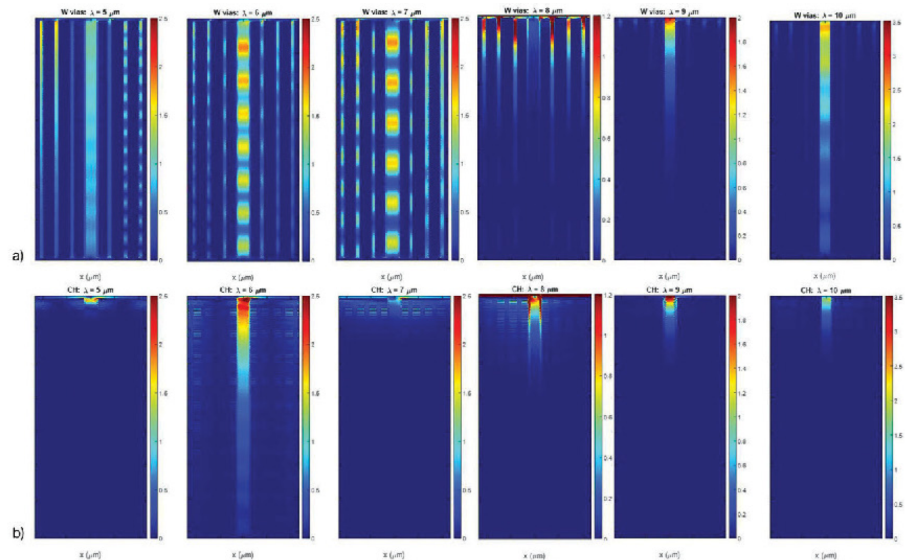
Figure 1. Large W vias replace the channel holes in the 3D NAND device in a specialized via to periphery (VtP) target.

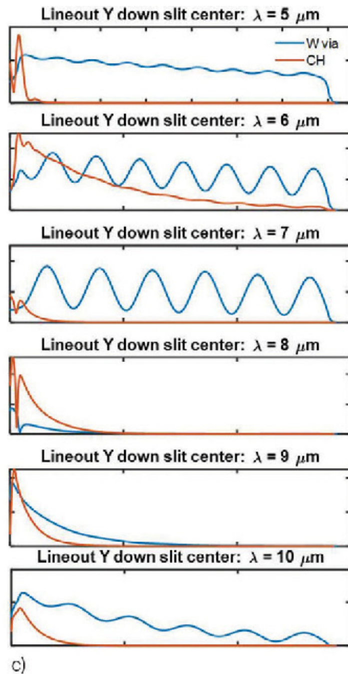
But before we discuss this new technique, we need to better understand plasmonics.

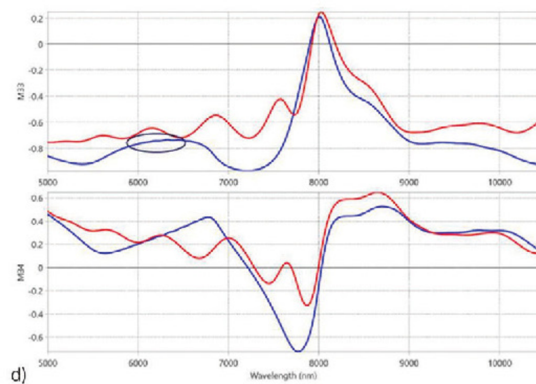
Understanding plasmonics

Plasmons are collective longitudinal oscillations of electrons in a plasma. Surface plasmon polaritons exist at the interface of a metal and dielectric and can be excited by photons if they are polarized in the plane of incidence and meet two other criteria. The first criterium that must be met is that incident photons and surface plasmon polaritons need to share the same frequency and momentum [3]. To match the frequency and momentum of the photon and surface plasmon polaritons, a coupling medium, like a prism or grating, must be used because a photon

Figure 2. (a) FDTD simulations of the VtP structure from wavelengths of 5 to 10µm at wavelength increments of 1µm and (b) FDTD simulations of 3D NAND device structure. (c) Electric field amplitude in the center of the wordline slit as a function of Z for VtP structure (blue) and 3D NAND structure (orange). (d) RWCA-based spectral simulations of VtP (red) and 3D NAND device (blue) structures with circled area corresponding to highly attenuated oscillations indicating the electric field penetrates to the bottom of the slit.







in free space has less momentum than a surface plasmon polariton. The second criterium is that the two materials must have opposite signs for the real part of the dielectric permittivity. Negative dielectric permittivity can be observed in metals and doped materials when the frequency is less than the plasma frequency. The dispersion relation relates the frequency of light to the spatial wavenumber of the surface plasmon polaritons and the equation for a single metal/dielectric interface system.

Simulations and motivation for target design

The plasma frequency is defined as when the real part of the dielectric function equals zero and becomes negative for lower frequencies [5]. For W, that wavelength is 942nm. IR light lower than this frequency can excite diffraction-assisted volume plasmonic resonance, following the metal gate replacement process step, in 3D NAND structures with wordline slit pitches less than one micron, allowing mid-IR light to reach the bottom of the wordline slit in the Z direction [6].

However, as 3D NAND scales, both wordline pitch and the number of tier stack pairs increase. This causes an exponential loss of sensitivity in the W recess despite the material's ability to support plasmonic resonance. Rigorous coupled wave analysis (RCWA) simulations run in Onto Innovation's proprietary Ai Diffract™ software in mid-IR demonstrate a decrease in sensitivity to the bottom W recess versus the wordline slit pitch by showing an increase in intrinsic uncertainty [7]. Further RCWA simulations were run in the software in the mid-IR region where Onto's Aspect® system operates (5 to 10.5µm) to validate the observation that an increase in wordline slit pitch reduces sensitivity to the bottom W recess.

Through-cell contacts were introduced to connect the lower metal layers below the array to the upper metal layers which are processed after the 3D NAND array is completed. This was done in conjunction with putting the peripheral circuitry under the NAND array. These through-cell contacts are large W vias (100s of nm in diameter), while the W vias are taller than the 3D NAND stack in the vertical direction and placed in the staircase region of the die. If these large W vias replace the channel holes in the 3D NAND device in a specialized via to periphery (VtP) target (**FIGURE 1**), they can act as a plasmonic waveguide and couple IR light, or more specifically wavelengths longer than the plasma frequency, to surface plasmon polaritons that can reach the bottom of the wordline slit.

Comparison of 3D NAND array structure to VtP target

To assess the feasibility of using a VtP structure as a plasmonic waveguide, FDTD simulations were

performed using the Lumerical™ FDTD software package on a 3D NAND device structure as well as a VtP structure with the same wordline slit pitch at the W recess step. RCWA-based spectral simulations were also run from wavelengths of 5 to 10.5µm. Both structures have 2XX layer pairs, a wordline slit pitch greater than 2µm, a slit width of roughly 250nm and a W recess of roughly 50nm. While the 3D NAND device structure has channel holes of roughly 100nm diameter between the slits, the VtP structure includes three W vias lined with SiO_2 and which have diameters greater than 250nm. Of these three vias, the central via is located at the half pitch, and the outer vias are located at roughly the quarter pitch of the structure.

FIGURE 2 (a and b) shows the results of the FDTD simulations for the 3D NAND device and the VtP structure from wavelengths of 5 to10µm in increments of 1µm. Fig. 2c shows a comparison of the electric field amplitude in the center of the wordline slit as a function of Z at the same wavelengths as Figure 2a. Figure 2d shows a comparison of RCWA-based spectral simulation of M33 and M34 components of the Mueller matrix for both structures from wavelengths of 5 to 10.5µm. The FDTD simulations show the amplitude of the electric field as it interacts with the structure.

The visible asymmetry in the electric field of the VtP structure is due to the oblique incidence angle of illumination and the phase difference induced by the distance between the source and the various apertures, which are the tops of the vias and wordline slit opening.

For the VtP structure, light can couple to SPPs and propagate through the wordline slit and SiO_2 liners to the bottom poly-Si layer at wavelengths of 5, 6, 7 and 10µm. At wavelengths of 8 and 9µm, the absorption of SiO_2 is largely due to the strong Si-O bond, causing

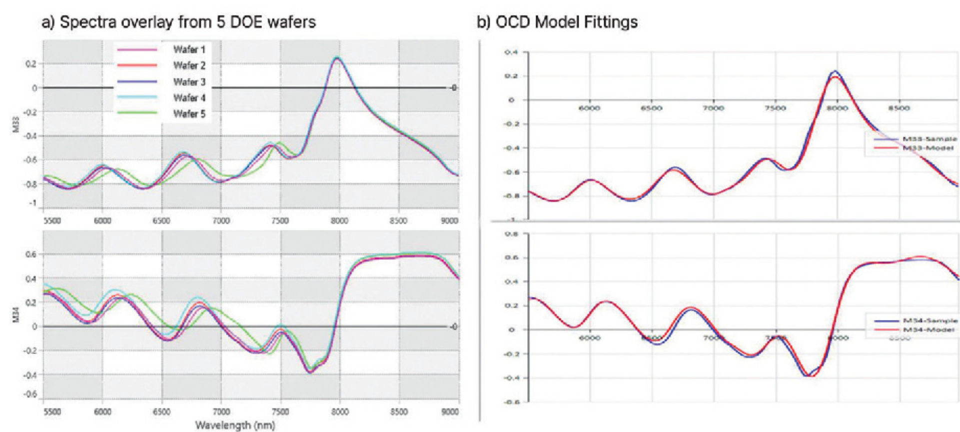


Figure 3. a) Mid-IR spectra overlay from five DOE wafers (one center site selected from each wafer) b) OCD model typical fitting.

the real part of the dielectric function to become negative, so that SPPs cannot be excited. SPP oscillations in the wordline slit are visible at wavelengths of 6, 7 and 10µm, and SPP oscillations are also apparent in the SiO_2 liner surrounding the W vias at a shorter wavelength compared to the slit region due to the smaller gap distance [3]. Fig. 2c and 2d show good agreement, indicating that FDTD simulations offer an accurate physical model of how SPPs propagate in the structures. Note that the electric field propagates to the bottom of the device structure at a wavelength of 6µm (shown in Fig. 2b and 2c), and it corresponds to highly attenuated oscillations in the simulated spectra from wavelengths of 6 to 6.5µm (circled in Fig. 2d).

Experimental results and analysis

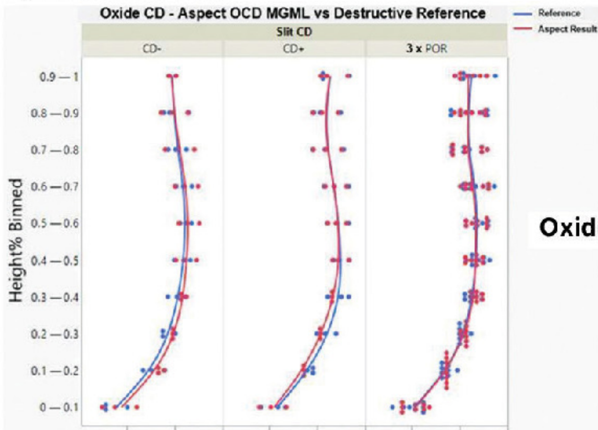
The proposed VtP structure was printed and processed as a scribe line target with a 2XX tier 3D NAND device process. Five wafers were prepared with a design of experiment (DOE) at three steps: – photolithography, dry etch and wet etch recess – to create skew on the slit CD, slit etch profile and W recess depth, respectively (Table 1). The wafers were measured on a mid-IR ellipsometer to get mid-IR spectra for the development of the optical critical dimension (OCD) model. Then we measured three sites on each wafer using a destructive reference tool to determine oxide CD and metal CD profiles. For each site, we measured over 130 positions from top to bottom. The average of each 10% height zone was used to optimize the OCD model.

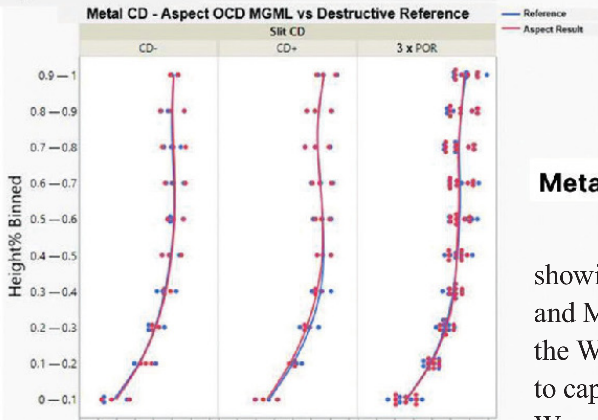
The spectra from the metrology system were then fit in the software. We used software embedded with machine learning to optimize the model and then used a model-guided machine learning (MGML) recipe to determine the results of the oxide CD and metal CD in the Z-profile. These results were then used to deduce the Z profile of the W recess.

Fourteen locations were measured with a destructive reference tool, and nine reference measurements were used for MGML training. The other five reference measurements were left to be blind tested to validate the robustness

Table 1. DOE on five wafers with skews from three process steps: photolithography, dry etch and wet etch recess.

WAFER	SLIT CD	SLIT ETCH	W RECESS
1	POR	POR	POR
2	POR	POR	Recess+
3	POR	POR	Recess++
4	CD+	ALT	POR
5	CD-	POR	POR





Oxide CD

Metal CD

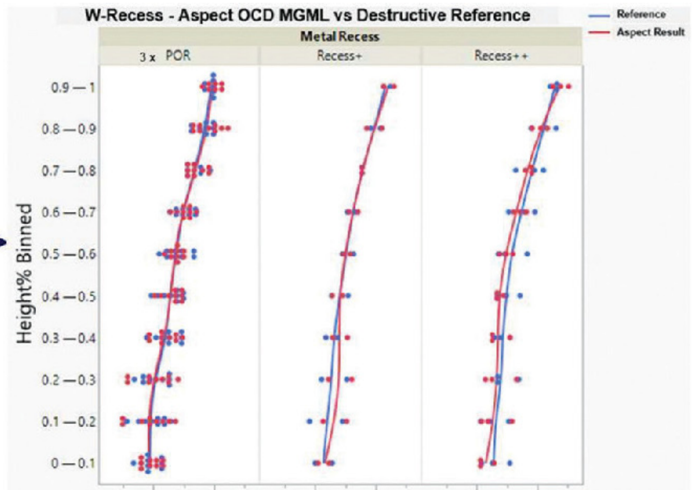
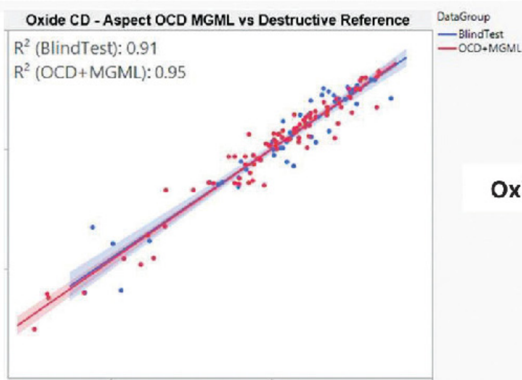
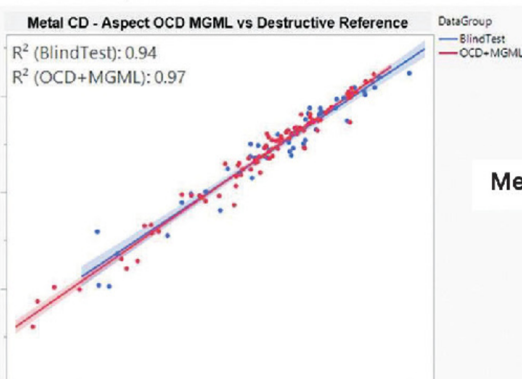


Figure 4. Side-by-side recipe result vs reference comparison for a) Oxide CD profile; b) Metal CD Profile; c) Deduced W recess profile.

of the recipe. The result of the OCD and MGML recipe is highly consistent with the references from the destructive tool, showing that not only is the OCD and MGML recipe able to capture the W recess skew, but it is also able to capture variations in CD and the W recess profile.

In **FIGURE 5**, each height zone from each site that has a reference as a data point was used to plot the recipe result versus reference correlation. Reference points used for recipe optimization are color-coded and labeled "OCD+MGML," while the blind test data are labeled "BlindTest." The R^2 for oxide and metal CD are high and consistently over 0.9 for both recipe optimization data and blind test data. For the W recess, the blind test is slightly lower, 0.79. However, it should be noted that we intentionally left recess skew edge sites for blind test as validation for robustness Continued on page 35





Oxide CD

Metal CD

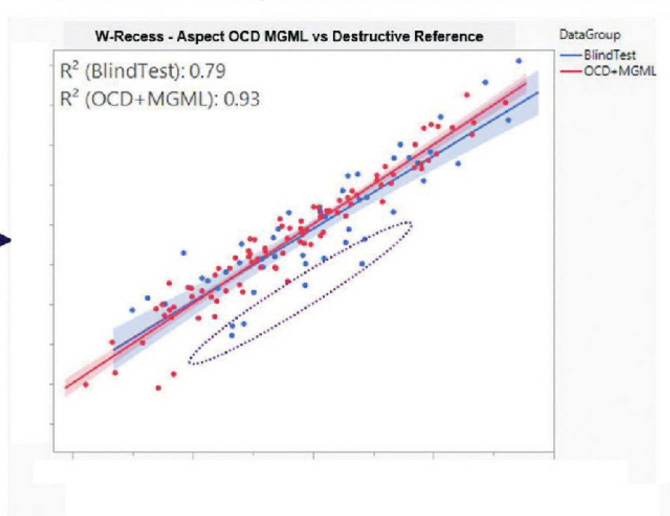


Figure 5. Recipe result vs reference correlation for a) Oxide CD profile; b) Metal CD profile; c) Deduced W recess profile.

to handle process variation since the edge sites have much larger process variation compared to all prior steps. The points that have larger correlation residue below the fit line were all from one site. If this edge site is excluded, the blind test R^2 will be over 0.85.

Conclusion

The tungsten recess replacement step is a key part of the 3D NAND manufacturing process. However, current metrology systems struggle to provide Z-profile measurements of this recess in HAR devices because channel holes are responsible for blocking the coupling of mid-IR light to SPPs in 3D NAND structures, which is likely caused by poly-Si channel material. The tech-nique outlined in this article of using a VtP structure, the wordline slit pitch and model-guided machine learning provides a way this important challenge can be overcome. Equally as important, this technique demonstrates the ability to recess skew and capture CD/recess profile variation for the entire W recess in HAR devices of 200 or more layers. This ability will be required for the high-volume manufacturing of bleeding edge 3D NAND devices.

About the author

Nick Keller has been with Onto Innovation since its founding in 2019 and prior to that Nanometrics, which merged with Rudolph Technologies to become Onto, since 2007. He has held many roles in Applications and Corporate Marketing. Keller has been instrumental in developing infrared critical dimension (IRCD) technology and providing pathfinding simulations in support of other new products at pre-initiation phases. He has four issued patents and over 20 publications. He received a Bachelor of Science in Electrical Engineering from the University of California Santa Barbara in 2007.

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