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Addressing Copper Clad Laminate Processing Distortion Using Overlay Corrections

By: Keith Best, Onto Innovation

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All great voyages must come to an end. Such is the case with our series on the challenges facing the manufacturing of advanced IC substrates (AICS), the glue holding the heterogeneous integration ship together.

In our first blog, we examined how cumulative overlay drift from individual redistribution layers could significantly increase overall trace length, resulting in higher interconnect resistance, parasitic effects and poor performance for high-speed and high-frequency applications. To address this, layer to layer overlay performance data needs to be monitored at each layer. If the total overlay error exceeds specifications at any process step, and at any location on the panel, corrective action must be taken to mitigate the drift in total overlay.

For this second installment, we explored the issue of AICS package yield and its importance in fostering a cost-effective, production-worthy process. Unlike most fan-out panel-level packaging (FOPLP) applications, AICS has relatively few packages per panel. This enormous disparity impacts yield calculations dramatically. In the AICS production process, the main challenge is the real-time tracking of yield for every panel, at every layer, throughout the fab. The solution: using advanced automatic defect classification (ADC) and yield analytics to quickly address errors.

In this final article of the series, we explore how overlay correction solutions compensate for panel distortion effects induced by copper clad laminate (CCL) processing, which impacts yield and final package performance.

Read on and enjoy the rest of the journey. Our port of call is ahead.

The Limitations of Large Landing Pads

CCL substrate processing requires the curing of build-up film, which is the dielectric material between the redistribution layers (RDL). During the build-up film curing process, the CCL substrate is subjected to repeated thermal cycling, resulting in the distortion of the X and Y coordinates of the interconnect patterns. This distortion impacts the registration of the laser-drilled vias to the lithography-printed RDL; this is known as layer-to-layer overlay.

The RDL design typically includes a large landing pad at the end of each interconnecting line/space (l/s) that connects to the vias. The landing pad is significantly larger than the critical dimension of the RDL. By including this feature, the overlay tolerance is increased significantly. For example, if the diameter of the laser-drilled via hole is 30µm, the RDL landing pad could be 50µm to provide an overlay tolerance of +/-10µm. With the interconnect technology roadmap approaching a point of inflection, from 12µm/9µm l/s to below 5µm/5µm l/s, it becomes increasingly difficult for advanced packaging designers to meet this

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challenge as the large landing pads limit design space. This results in the need to increase the number of RDL layers, along with a commensurate increase in cost and potential yield loss. To mitigate this design quandary, smaller RDL landing pads are required, which can only be achieved if the process overlay is improved.

With improved overlay performance, RDL and via structures with smaller landing pads can be squeezed into a smaller area, eliminating the need for additional RDL layers. Moreover, this reduces the cost and the yield loss risk.

Distortion Errors
To improve process overlay, the lithography system, or stepper, must analyze and compensate for CCL substrate distortion errors. This sounds simple in principle; however, the CCL distortion components are complex and extend beyond the traditional six (6) parameter model supported by most lithography steppers. This non-linear distortion requires additional higher order lithography system corrections, increasing the complexity of the model.

The stepper's ability to correct for the substrate distortion is only part of the solution. We also need accurate metrology data to generate the optimum alignment solution to compensate for distortion errors. This data is typically available after the lithography process is completed and overlay of the vias to RDL landing pad is measured. The data is then analyzed and sent back to the stepper to correct panel distortion for future incoming panels. These are known as feedback corrections. This after-the-fact data is only relevant if the panel distortion remains constant for incoming future panels. Of course, sampling plans and periodic metrology can help generate a run-to-run solution. With this, AI and machine-learning software can correct the dynamic distortion errors exhibited by CCL substrates over time. An alternative approach could be to gather metrology data from the substrates after the laser-drilled vias have been created, prior to their arrival at the stepper. These are known as feedforward corrections.

Feedforward metrology requires a leap of faith since it depends on the laser-drilling tool and stepper working in concert to produce an accurate and reliable data set to create the stepper alignment solution. (Figure 1)

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Overlay Solution for AICS Panels

Enhance Manufacturing Productivity with Process Analytics

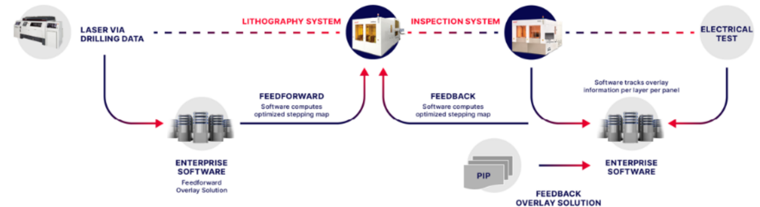

Figure 1: Overlay solution for AICS panels

In principle, the ideal solution to solve the overlay problem would be to use a feedforward approach, where X and Y co-ordinate data from the laser-drilled via holes are employed to generate an alignment solution. Of course, overlay metrology will confirm if the feedforward correction is accurate and will highlight the residual errors. If the residual errors are significant, it suggests that the feedforward model needs to be adjusted. Ironically, post-exposure, final overlay metrology could be used to optimize the feedforward model. With continued iterations, in conjunction with machine learning, the model could be continuously adjusted to achieve good overlay with low residuals.

Conclusion

The manufacturing of large packages requiring the heterogeneous integration of chiplets, HBM and GPU/CPU is only achievable using AICS processing. To deliver this capability, substrate distortion needs to be characterized and compensated for to maintain high yields and reduce costs. A comprehensive metrology and lithography solution is required. This solution should be used in conjunction with advanced software that can automatically adjust models to compensate for the dynamic substrate distortion components. This approach, and the ones outlined in our previous blogs in this series, could extend the roadmap of CCL substrate manufacturing beyond its current design limits, reducing costs, improving yields and ensuring a smooth-sailing future for heterogeneous integration applications.

About the author

Keith Best is the director of product development, lithography, at Onto Innovation. If you would like to know more about Onto's lithography solutions, please visit our site.