Achieving Zero Defect Manufacturing Part 1: Detect & Classify

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Whether the discussion is about smart manufacturing or digital transformation, one of the biggest conversations in the semiconductor industry today centers on the tremendous amount of data fabs collect and how they utilize that data.

While chip makers are accumulating petabytes of data across the entire semiconductor process, a question arises: how much of that information is being fully utilized? The answer may be around 20%, according to the Semiconductor Engineering article "Too Much Fab and Test Data, Low Utilization." Unfortunately, this poses a challenge because fab end customers are demanding highly reliable chips, in other words, chips with zero escaping defects and which offer manufacturers clear genealogy and traceability.

Many of you reading this work for companies that have started or are planning digital transformations. To do this, these companies will need to better integrate the data they collect — and that includes data from materials, products, processes, factory subsystems and equipment.

For smart manufacturing to truly live up to its potential, manufacturers will need inline automation that takes complete advantage of the analytics their monitoring systems generate, analytics which can be fed back to the process tools, manufacturing execution systems and other factory systems in real time. Working in concert, these integrated systems are essential to creating a zero defect manufacturing environment.

In the world of smart manufacturing, manufacturers will be tasked with providing timely total solutions to detect and classify defects using inspection and metrology tools, conduct root cause analysis to determine the source of said defects and, finally, employ process control and equipment monitoring using run-to-run and fault detection and classification software solutions to prevent defects from reoccurring.

In this blog, the first in our three-part series "Achieving Zero Defect Manufacturing," we will focus on detecting and classifying defects. We will start by looking at solutions at the defect level before moving on to the die level and the wafer level.

Defect Level

Today, a fab might deploy, across the factory, several different inspection and metrology tools from several different vendors, including automated optical (AOI) tools, optical scanning electron microscopes (SEMs) or even cameras. Each one of those tools comes with their own learning curves and unique operational features.

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To further complicate matters, many of today's chips and packages require inspection solutions capable of detecting critical defects at ever smaller resolutions. And therein lies the problem: AOI tools running at higher sensitivities often result in excessive rates of nuisance, non-visual defects and noise, a complication that is further exacerbated by increases in density. In some cases, this excessive noise can make the entire inspection process ineffective.

By using metrology and inspection tools integrated with an AI-based automatic defect classification (ADC) system, manufacturers can employ on-the-fly strategies to detect defects and classify them. With a real-time approach, fabs can reduce the noise and their impact to yield by up to 60%, based on feedback Onto Innovation has received from customer validations.

Another challenge that traditional defect inspection presents comes from the use of manual review stations or offline review software, in which inspectors pick up wafers and physically inspect the wafers using optical microscopes or review defects using offline review software. Not only is this time consuming, there are human errors and inconsistencies wherever a person is involved. And so what smart manufacturing needs is to eliminate manual review stations. With a single ADC platform capable of automatically inspecting the entire wafer — front, edge and backside — this process is significantly improved. This is another area where using the same ADC platform is beneficial to the zero defect manufacturing process in finding multiple anomalies.

In addition, if a customers chooses to use a single ADC system, they no longer have to learn how to use multiple ADC, one each, possibly, from a different AOI vendor.

Be that as it may, AI-based platforms need to be balanced and offer higher classification, accuracy and purity rates. To address this challenge, manufacturers should adopt a multi-engine approach.

With a multi-engine approach, chip makers can use different algorithms to classify defects. As a result, manufacturers have the ability to align these engines and ensure the classification accuracy is there. When different engines don't align with the classification, manufacturers can classify them as unknowns and feed that back to operator classification.

Die Level

Now that we have discussed challenges and solutions at the defect level, we will examine the next level of detection classification, the die level. At the die level, there may be multiple defects and anomalies. With that in mind, chip makers looking for defects at the die level can

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apply automatic die binning rules, such as the good die in the bad neighborhood rule.

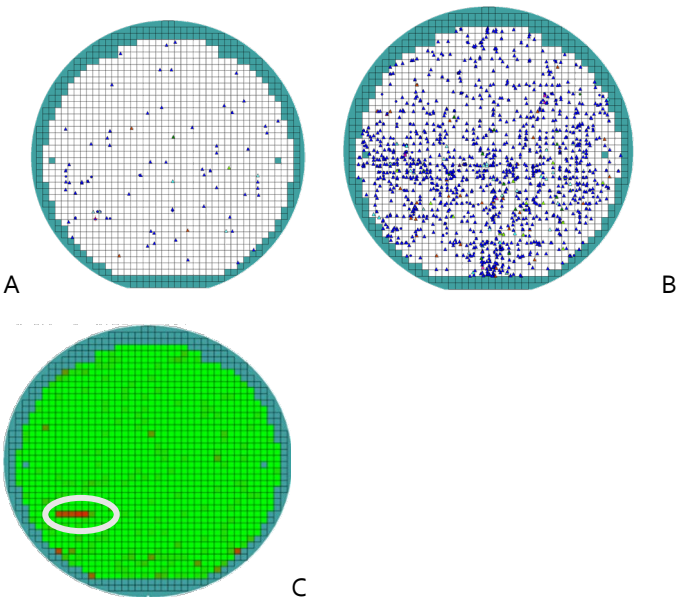

Figure 1: Defect map (a), stacked map (b) and stacked probe map with a micro crack (c)

In Figure 1 we present a single wafer defect map, lot stack defect map and lot stack probe bin map. In the map for a stacked probe map with a micro crack (Fig 1c), the red dies indicate the frequency of the dies across the entire lot that have failed.

If you look at the individual defect map (Fig 1a) or lot stack defect map (Fig 1b), there is a risk that both inspection tools and operator review might miss classifying micro crack die failures as shown in the wafer probe lot stack of die bin results. However, using auto die binning rules, it is possible to fully bin an entire region to proactively avoid latent defective dies going into the back end. Inspectors can even expand the binning rules to the surrounding dies, proactively killing them during the review step or post inspection.

Wafer Level

With both the defect and die level out of the way, the next level we will look at is the wafer level. This is where you might find multi-die wafer level systematic issues such as scratches or clusters of bad die.

At Onto Innovation, we have noticed that 21% of wafer starts have some form of wafer level signature, whether it is a small cluster, a big cluster or unknown issues, according to two papers we co-authored. So

having a machine-learning module capable of detecting these types of patterns on the entire wafer is beneficial. With such an approach, manufacturers can conduct inline wafer level monitoring, thereby enabling them to bin the defects in the pattern, dies with the patterns and the wafers. This will avoid time-wasting rework and take action to prevent these signatures.

Furthermore, we have discovered that a small percentage of the data generated using the approach outlined in this blog is of unknown new patterns. In these cases, manufacturers can apply the same machine-learning algorithms and identify a pareto of similar unknowns and then use that information to add to the pattern library for monitoring.

Conclusion

Achieving zero defect manufacturing is not just an admirable goal for chip makers, it may soon become a necessity. However, there are solutions that can make reaching this goal a reality. By better utilizing the massive amounts of process control data at their disposal, along with an ADC platform, manufacturers can better classify defects at the defect, die and wafer level in real time and make process corrections so that bad die will not advance to the next stage of the process, thereby bringing factories closer to zero defect manufacturing. At Onto Innovation, we have explored this topic extensively and have come up with solutions to these challenges.

In our next blog, we will dive further into the subject of zero defect manufacturing as we look at root cause analysis. We hope you will join us.

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