Front-end Technologies Are the New Back-end Tools: Using Picosecond Ultrasonics Technology for AI Packages, Part 1

By Cheolkyu Kim,
Onto Innovation

Content as published on
Semiconductor Engineering blog post, June 2025.

If you are a part of the semiconductor industry or simply someone interested in the field, you have likely heard what has become a common refrain: the back-end of the process is becoming more like the front-end of the process. In other words, the technologies that were once exclusively deployed in the first part of the process are being used to meet the increasingly stringent requirements of advanced packaging on the back of the process.

This is especially true for complex AI devices, where heterogenous integration brings together multiple chips with different functionalities. These devices present manufacturers with new interconnect challenges, especially when it concerns redistribution layers (RDL) and bond pads. This is certainly the case for high-bandwidth memory chips, some of which may feature eight to 12 interconnected DRAM chips. And those numbers are only going to climb higher, while the need to properly measure interconnects is only going to grow in importance.

With RDL and bond pad metrology, the need to measure sites under 10µm is emerging as a new requirement. Unfortunately, traditional back-end approaches – like X-ray fluorescence or sheet resistance measurements and white light scanning interferometers – have limited capabilities that make them poor candidates for advanced interconnect process control. Measuring RDL and bond pads in AI packages requires traditional front-end metrology tools offering in-line process control capable of measuring small sites within a tight process control window (Figure 1).

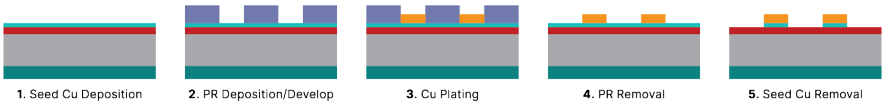

Figure 1: The process flow for RDL formation.

The semiconductor industry has long adopted picosecond ultrasonic technology as a non-contact, non-destructive technique capable of providing accurate measurements for single-layer and multi-layer metal films. Recently, Onto Innovation and Samsung Electronics Co., Ltd., teamed up to explore how this front-end mainstay also could be used to measure metal thickness in RDL and bond pads in high performance AI packages.

In part one of this two-part blog series, we will focus on traditional techniques and current challenges, whereas in the second blog we will discuss solutions involving picosecond ultrasonic technology. But first, a

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quick word about the latest generation of picosecond ultrasonic technology.

Picosecond Ultrasonic Technology

In our study, we used fifth generation picosecond ultrasonic technology to measure the thickness of individual metals on multi-layer structures. To measure very rough film, pump beam intensity was modulated at 5 MHz. This modulates the intensity of the acoustic wave it generates. Then the reflected probe beam signal from the detector was demodulated with the same frequency as the pump modulation, allowing for the measurement of weak reflectivity changes caused by the acoustic wave.

As the pump beam itself does not convey any information about the travelling acoustic wave but has the same frequency as demodulation, demodulating the signal from the detector may include the signal from the pump, resulting in significant noise. This is especially the case when measuring rough films where pump beam scattering is strong. To address this, such noise can be filtered out by modulating the probe beam at a different frequency, 0.5MHz, and demodulating the signal from the detector with the sum of the two frequencies, 5.5 MHz. Another significant improvement made to this technology is that the maximum probe beam time delay for the measurement has increased from 5 nanoseconds (ns) to 15ns. This means the maximum thickness that can be measured has increased threefold. For Cu measurement, the maximum thickness that can be measured is now 35µm.
With our discussion of picosecond ultrasonic technology out of the way, we will turn our attention to the advanced packaging needs of AI devices.

AI Packages

To create AI devices, manufacturers use heterogeneous integration to package memory and process chips together in 2.5 and 3D structures. This enables faster communication and lower power consumption.
In these structures, conventional memory chips are replaced with high bandwidth memory (HBM) and paired with a graphics processing unit (GPU). HBM enables the higher data transfer rates needed to handle the significantly increased data processing generated by parallel computation with the GPU. In the latest generation HBM, eight to 12 DRAM chips are connected to each other vertically by through silicon vias (TSV) to form one HBM package. Then four to six HBM packages are connected, horizontally, with the GPU chip by RDL on a Si interposer. These new interconnected structures offer significantly improved computing power and latency and higher bandwidth for data

transfer and low power consumption. Each are needed for AI computing.

In the case of RDL on a Si interposer, manufacturing multiple layers of RDL is required to handle high data transfer rates. As such, the manufacturing process is more complex compared to the manufacturing process for mature packages.
Metals, mostly Cu, in RDL are typically deposited using the electroplating (EP) process. The thickness of the metals is affected by the geometric structure underneath, making thickness uniformity control very challenging. To meet the within wafer uniformity requirement for RDL impedance control, measuring and monitoring metal thickness directly on product wafers is crucial. As RDL lines shrink to 2µm or lower – the line/space (L/S) requirements of the most advanced packages – dimensional control is vital to device performance while process control itself becomes even more stringent.

After the final RDL layer on a Si interposer is formed, bonding pads are created. These bonding pads connect with HBM or GPU chips through micro-bumps. Like RDL, bonding pads are also created using the EP process. However, some bonding pads are flat while others possess a dimpled structure (Figure 2). To maintain process control, engineers will still need to measure metal thickness directly on both flat and dimpled structures. In the case of the latter, such measurements are a lot more challenging.

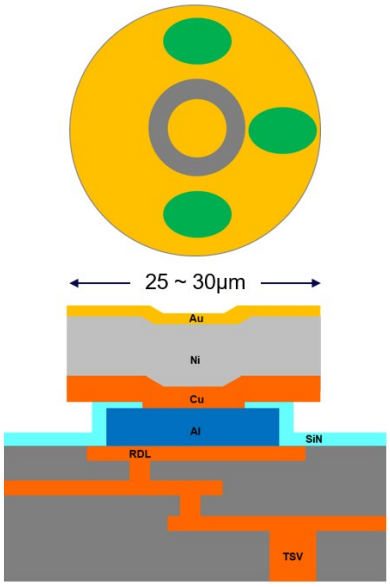

Figure 2: The schematic for a bond pad with a dimple structure.

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Traditional Packaging Process

During the traditional packaging process, metal film measurements are characterized using automated and semi-automated measurement tools such as X-ray fluorescence or sheet resistance measurements. While these tools are easy to use and offer low cost of ownership, they are not up to the task of measuring multi-layered films or films with varying topographies on product wafers in high volume manufacturing. White light scanning interferometer (WLSI) systems are also used in RDL process monitoring. These methods rely on wavelength-dependent interference patterns to provide the step height of metals; this assumes that the step height is the same as metal thickness, which may or may not be true depending on the structure.

As RDL films become thinner, wavelength dependent interference patterns become less sensitive to thickness variation. This affects measurement accuracy. In the case of RDL lines 2µm L/S and lower, the accuracy of thickness measurements becomes even more critical for process monitoring and control. However, WLSI systems have shown limitations in meeting these metrology requirements.

In general, the front-end process must operate inside a window that varies within 10% of the target value. This, in turn, requires a metrology tool with a gage capability (3σ repeatability and reproducibility) of 10% of the variability or 1% of the target value. This metrology tool must be able to measure in-die areas and on test structures smaller than 50µm on real product wafers. Such a tool also needs to be non-contact, non-destructive and fast enough to support high volume production. Picosecond ultrasonic technology enables advanced packaging manufacturers to meet these challenges.

In our next blog, we will take a deep dive into how picosecond ultrasonic technology can be used to measure metal films during RDL and bond pad processes. We hope you join us as we continue to explore the advanced packaging applications of picosecond ultrasonic technology.

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Acknowledgments
We would like to thank Dae-Seo Park, Sanghyun Bae, Junghwan Kim, and Hwanpil Park of Samsung Electronics Co., Ltd., and Kwansoon Park, G. Andrew Antonelli, Robin Mair, Johnny Dai, Manjusha Mehendale and Priya Mukundhan of Onto Innovation for their contributions to this article.

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Cheolkyu Kim, Ph.D., is director of product marketing at Onto Innovation with a focus on application development for picosecond ultrasonic (PULSE™) and inspection technologies. Prior to joining Onto, Kim was a postdoctoral research associate in the Physics Department of Brown University. During his three years at Brown, he spent time researching magnetically levitated superfluid liquid helium.