Addressing Trench Structures and Larger Wafers for Power Devices

By: Vamsi Velidandla,
Onto Innovation

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Wind power. Rail. Solar energy. And, perhaps most significantly, electric and hybrid vehicles. Together, these four forces are among the major demand drivers for power devices.

While silicon (Si) still plays a role in power devices, wide-bandgap compound semiconductors like silicon carbide (SiC) and gallium nitride (GaN) are particularly well-suited for power devices thanks to their higher electron mobility, higher critical electric field and higher thermal conductivity. However, as new structures and larger wafer sizes become the norm for power devices, they bring with them distinct manufacturing challenges.

Today, the industry is transitioning from 150mm to 200mm wafers for SiC- and GaN-based devices and 200mm to 300mm wafers for Si-based devices. The reason: larger wafer sizes may help reduce the cost of fabrication. As the wafer size transition occurs, it is important to have a metrology tool that can measure a larger number of data points across the wafer without impacting the overall fab throughput. A loss of throughput adds to cost-of-ownership and may erase savings earned from transitioning to larger wafers.

First of all, let's further examine one of the challenges posed by the transition from 150mm wafers to 200mm wafers: within-wafer variation. For reasons that are immediately obvious, larger wafers have more within-wafer variation and, therefore require more points of measurement per wafer, especially at the outer edges where yield is often lower.

Consider a metrology tool designed for 150mm wafers: it can measure five points on the wafer. But with a 200mm wafer, measuring only five points will leave a number of blind spots, areas where there might be significant within-wafer variation. For proper measurements of a 200mm wafer, more measurement points — 13 in some cases — are needed to generate an accurate view of within-wafer uniformity.

There is yet another process control challenge to consider when it comes to compound semiconductor power devices: the adoption of trench-based structures (Figure 1). Moving from planar to trench-based structures enables reduced on resistance (R_{on}). The move to trench-based devices makes the measurement of trench characteristics like top critical dimension (CD), bottom CD, sidewall profile and corner rounding important criteria in the device flow. Device manufacturers need to be certain that each trench on every die on every wafer is within control limits so that device performance over the whole wafer, and from wafer to wafer, is within specifications.

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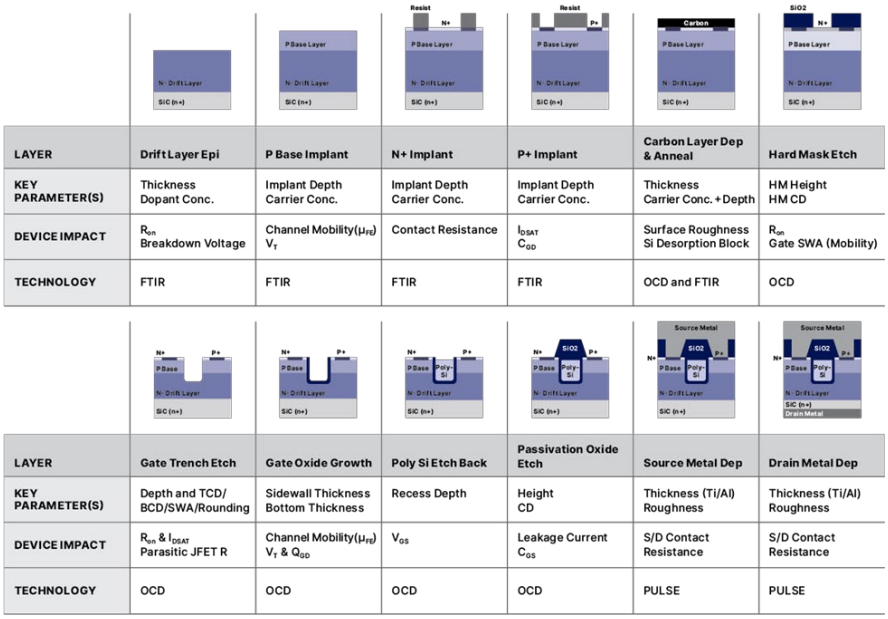

LAYER	Drift Layer Epi	P Base Implant	N+ Implant	P+ Implant	Carbon Layer Dep & Anneal	Hard Mask Etch
KEY PARAMETER(S)	Thickness Dopant Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Implant Depth Carrier Conc.	Thickness Carrier Conc. + Depth	HM Height HM CD
DEVICE IMPACT	R_{on} Breakdown Voltage	Channel Mobility(μ_{FE}) V_T	Contact Resistance	I_{DSAT} C_{GD}	Surface Roughness Si Desorption Block	R_{on} Gate SWA (Mobility)
TECHNOLOGY	FTIR	FTIR	FTIR	FTIR	OCD and FTIR	OCD

LAYER	Gate Trench Etch	Gate Oxide Growth	Poly Si Etch Back	Passivation Oxide Etch	Source Metal Dep	Drain Metal Dep
KEY PARAMETER(S)	Depth and TCD/ BCD/SWA/Rounding	Sidewall Thickness Bottom Thickness	Recess Depth	Height CD	Thickness (Ti/Al) Roughness	Thickness (Ti/Al) Roughness
DEVICE IMPACT	R_{on} & I_{DSAT} Parasitic JFET R	Channel Mobility(μ_{FE}) V_T & Q_{GD}	V_{GS}	Leakage Current C_{GS}	S/D Contact Resistance	S/D Contact Resistance
TECHNOLOGY	OCD	OCD	OCD	OCD	PULSE	PULSE

Figure 1: The SiC trench MOSFET process.

In specific regard to SiC trench-based MOSFETS, it is particularly important to monitor corner rounding so as to reduce the localized electric field density, thereby avoiding potential device breakdown.

In D-mode GaN high electron mobility transistor (HEMT) devices, the source/drain (S/D) recess etch of the top AlGaN layer must land on the 2D electron gas (2DEG) region. After this etch, the S/D contact metal deposition consists of a multi-metal stack. The etch needs to be optimized so that the bottom of the trench exposes the maximum surface area of the 2DEG layer. Any depth variation will lead to increased contact resistance. Therefore, accurately controlling the trench depth in the AlGaN layer is important to ensure optimized contact of the S/D metal stack with the 2DEG layer, thereby enabling the lowest device on resistance.

Given these new power device challenges and others, it is no wonder that manufacturers of trench-based power devices are looking to adopt inline process controls at several key steps, such as trench formation, poly deposition and gate formation, while larger sizes — 200mm wafer for SiC and 300mm for Si — require more points on the wafer to be measured.

Conclusion

The transition from 150mm to 200mm wafers for SiC- and GaN-based power devices, and from 200mm to 300mm for Si-based power devices,

is underway for some manufacturers and on the horizon for others. Both SiC and GaN device types will be required for specific applications as more automakers transition to hybrid and full battery electric vehicles. Consider these figures from the Yole Group: SiC and GaN power devices are experiencing an annual average growth rate approaching 34% and 44%, respectively, through 2027.

Faced with these challenges, and the growing demand for compound semiconductor power devices, the need for a single tool to conduct thin film and OCD measurements for power devices is key to maintaining throughput while preserving the benefits of new structures and the potential cost-savings of larger wafer sizes.

In part two, we'll go into detail about getting the most out of these processes as power device manufacturers transition from 200mm to 300mm wafers.

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