Addressing Total Overlay Drift in Advanced IC Substrate (AICS) Packaging

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For years, many in the semiconductor industry have focused on the march toward advanced nodes. As these nodes have decreased in size, the size of input/output (I/O) bumps on the chip has grown smaller. As these bumps shrink, their ability to mate directly to printed circuit boards (PCB) diminishes, which, in turn, leads to the need for an intermediary substrate. Enter the advanced IC substrate (AICS).

The use of AICS also enables advances in panel-level packaging and the rise of chiplet-based architectures, where the final product is an assembled composite of multiple die supporting the core central processing unit (CPU) or graphics processing unit (GPU). These additional die may be memory elements, analog devices or other functions. All these die can be co-packaged on the AICS, which allows multiple die with small I/O contacts to be assembled and redistributes them to larger contact bumps compatible with a PCB.

With panel-level packaging, manufacturers can deliver packages offering faster data transfer, greater heat dissipation, less power consumption and increased functionality. And unlike the front-end where higher resolution involves ever smaller patterns, package sizes are only increasing in size.

Further complicating matters, these packages also feature elevated numbers of redistribution layers (RDL) to improve input/output (I/O) count and functionality. As the number of RDL layers increases, we are presented with a number of challenges, including achieving smaller resolution requirements and minimizing overlay errors, the latter a particular pain point facing the RDL process.

While we tackled resolution and overlay drift in previous blogs on panel-level packaging, we haven't addressed the challenge of what is called "total overlay" drift and the solutions that can help manufacturers solve this, frankly, all-but-certain issue.

But before we get into that, let's talk about how RDL processing affects the substrate.

The AICS process flow requires the curing of Ajinomoto build up film (ABF) after each via layer is laser drilled. This continuous thermal cycling of the copper clad laminate (CCL) substrate and dielectric, together with the increasing number of RDL layers, distorts the substrate. This non-linear distortion results in each quadrant of the panel having vastly different overlay results when a global alignment solution is applied. In particular, this is a high-throughput challenge for lithography systems employing extremely large exposure fields (250 mm x 250 mm) and which are capable of exposing a panel with only four (4) shots.

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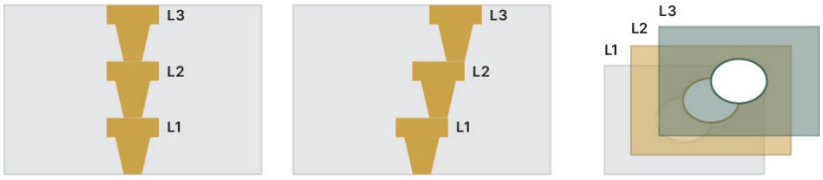
The number of RDL interconnect layers is typically between five (5) and 12 layers per side connected by a plated through hole (PTH). The resulting RDL stack could contain up to 24 layers of layer-to-layer overlay errors. For AICS, the overlay requirements go beyond the challenging layer-to-layer specifications; they are for the entire RDL stack. The total overlay is the summation of the overlay errors for all RDL layers, with respect to the last layers on either side of the panel. Cumulative overlay drift from individual RDL buildup layers could significantly increase overall trace length, resulting in higher interconnect resistance, parasitic effects and poor performance for high-speed and high-frequency applications.

The layer to layer overlay performance data need to be continuously monitored at each layer as the summation continues through the film stack. If the total overlay error exceeds specification at any process step, and at any location on the panel, the excursion needs to be flagged so that the necessary corrective action can be taken to mitigate the drift in total overlay. This is important to prevent RDL from exceeding the design resistance specifications for a package.

For instance, if the overlay drifts 5µm per layer, and there are 10 layers, the total RDL length will increase by 45µm which will impact the overall RDL resistance. Of course, this problem is exacerbated as the number of layers increases, i.e., in a 24-layer RDL stack the interconnect length would increase by 115µm.

In order to address the total overlay challenge and provide visibility of the layer-to-layer dynamics as the number of process layers increases, an overlay tracking system is required, one that incorporates metrology, lithography and analytics. This system needs to record measurements for every RDL-to-via overlay across the entire panel and to continuously sum the vectors, from layer to layer, as the process stack increases.

One such system could use inspection and data analytics to track and compensate for multi-layer overlay drift. An error signal would be generated when the cumulative overlay error exceeds a user-defined threshold. The required overlay correction offsets would then be calculated and sent to the lithography system. Without the ability to monitor the summation of overlay errors across the panel, and layer to layer, there is no way to know until final e-test if RDL resistance meets specification.



OPTIMAL INTERCONNECT STACK

"TOTAL OVERLAY" ERROR OF STACK DRIFT, RESULTS IN INCREASED INTERCONNECT RESISTANCE

PLAN VIEW

As RDL dimensions continue to shrink, this issue is going to become increasingly important. Moreover, the ability to visualize and flag excursions and trends provides the manufacturing team with an early warning that there may be trouble ahead and offers them the opportunity to take corrective action before the substrates are unrecoverable and scrapped at e-test. This ability is vital for manufacturing processes involving multiple stacked RDL structures.

In the next blog in this series, we will move beyond total overlay and focus on improving yield during AICS panel-level packaging processes. For AICS processes, the increasing package size limits the number of packages per panel, making high yield even more challenging. A single killer defect can cause an entire package to fail at e-test. This will have a significant impact on yield percentage, and, with so many layers of RDL, every layer becomes even more critical. We hope you will join us.

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