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Addressing Yield Challenges in Advanced IC Substrate (AICS) Packaging

By: Keith Best, Onto Innovation

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No matter how you get your news, it seems like everyone is talking about AI – and it's either going to usher in a new era of productivity or lead to the end of humankind itself. Regardless, the AI era is here, and it's just beginning to have an impact on our lives, our jobs and our future.

To meet the rigorous demands of AI – along with high-performance compute, 5G and electric vehicles – the semiconductor industry is seeking out new innovations to increase speed, bandwidth and functional density, lower energy usage, cost and latency. At the top of the list: heterogeneous integration. And to make heterogeneous integration a reality, back-end packaging houses use advanced integrated circuit substrates (AICS).

In a previous blog, we focused on one of the major challenges of manufacturing AICS – total overlay drift. For this second installment in our three-part series on packaging solutions, we explore the issue of AICS package yield and its importance in fostering a cost-effective, production-worthy process.

For starters, AICS yield challenges are unique in the semiconductor industry. Unlike most fan-out panel-level packaging (FOPLP) applications, where package sizes are typically less than 10mm x 10mm and the number of packages per panel are in the thousands, AICS has relatively few packages per panel. For example, a 510mm x 515mm AICS panel can only accommodate 16 packages (120mm x 120mm) compared to FOPLP, which could have over 2,300 packages. This enormous disparity impacts yield calculations dramatically; one defective package on an AICS could result in a 6.25% yield loss, whereas with FOPLP, one defective package may only represent a 0.04% yield loss. As the AICS package size increases to 150mm x 150mm, the yield challenge is exacerbated: a single defective package failure results in an 11% yield loss, a significant yield decrease in an industry that operates under extremely narrow margins.

With AICS, the opportunities for yield loss are significantly higher than for FOPLP, especially from a defectivity perspective. After all, there are many more process layers with AICS compared to FOPLP. AICS designs can have up to 24 redistribution layers (RDL), split between the frontside and backside of the substrate, whereas FOPLP typically has only three to five RDL layers.

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In addition, processing both the frontside and backside of the AICS is another unique process requirement that significantly increases the risk of yield loss from defects caused by surface contamination.
In the AICS production process, the main challenge is the real-time tracking of yield for every panel, at every layer, throughout the fab. The motivation for this ongoing yield assessment is to determine the optimum fab loading to meet productivity targets. It takes a few weeks to complete the processing of an AICS, and only by knowing the yield of an entire fab's AICS inventory, in real-time, will productivity be evaluated accurately. Furthermore, panel yield needs to be assessed in terms of cost, at each process step. For example, if a panel has a yield of 50% and it is only at layer five in a 40-layer process, is it worth processing the panel further? Should the panel be scrapped and restarted? The answer is often yes.

The AICS process is a die-last process, so the panel is not of high value until the die are placed at the very end of the build. In the case of AICS fabrication, knowing when to scrap, restart or continue to process low-yielding AICS becomes a business decision, one that relies heavily on accurate yield data. Of course, the yield loss needs to be investigated and root causes identified as soon as defects, both potential and actual, arise. This is where the use of advanced automatic defect classification (ADC) and yield analytics are imperative for a quick and successful recovery.

To track the panel yield, a comprehensive and intelligent yield-tracking database is required. This database must have access to inspection data for each panel at each process step. In addition, the inspection data must have an ADC system that has been trained to identify killer defects. These killer defects, such as RDL opens, RDL shorts, missing vias and via residue, must be classified with 100% accuracy, so that each defective package on the panel can be identified with confidence. The yield-tracking database must also provide the user with signals to stop the production line if yield drops below a user-defined threshold. Furthermore, some defects may not be apparent until later in the process. For instance, a large particle embedded in the Ajinomoto build-up film (ABF) may not impact the current via layer, but a later RDL pattern that is located on top of the particle could induce RDL bridging due to the particle creating an out-of-focus lithography condition.

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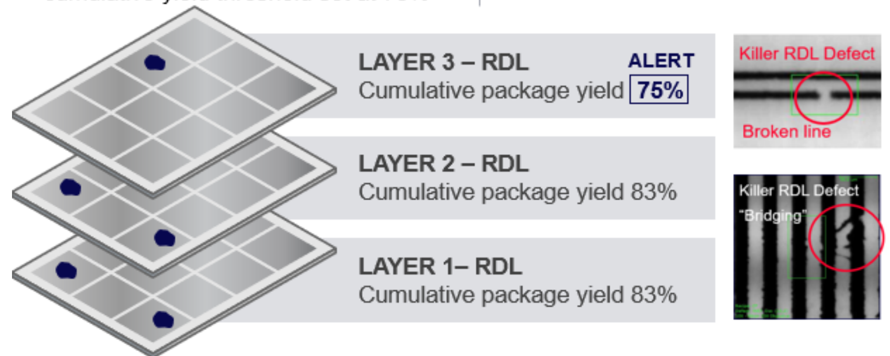

As the industry transitions to glass core substrates, which may allow for single-side processing, future AICS processes may become more robust. However, package sizes will continue to grow, and RDL will continue to shrink below a line/space of 5µm. This technology roadmap will require new photoresist and photo imageable dielectric processes. ABF will no longer be capable of supporting less than 10µm vias with laser drilled vias.

For AICS processing, yield is critical, and more challenging than traditional FOPLP. The rapid increase in demand for AICS, larger package size and increasing number of layers drives the urgency for accurate ADC inspection and yield analytics. Ramping up AICS manufacturing in a timely manner and maintaining cost effective productivity cannot be accomplished without leading-edge advanced packaging inspection and yield management systems.
Please join us for part three of our solutions series where we discuss AICS overlay correction solutions.

About the author
Keith Best is the director of product development, lithography, at Onto Innovation. If you would like to know more about Onto's lithography solutions, please visit our site.