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A Bare Wafer Mystery: Inspecting for Back, Edge and Notch Defects in Advanced Nodes

By: Burhan Ali,
Onto Innovation

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It is no mystery that the semiconductor industry is always advancing, with specifications becoming increasingly stringent as defects become increasingly more difficult to discover. This is especially true in the case of the most advanced nodes, where ever-smaller flaws and deformities can result in a killer defect.

To solve this More than Moore mystery, you do not need to employ the detective skills of Sherlock Holmes. You need the metaphorical equivalent of the pipe-smoking hero's magnifying glass to find the particles, scratches, pits and air pockets hiding in the shadows.

Take the critical dimensions of trenches and vias, for example. As they shrink, the size of a particle or scratch that can potentially result in a killer defect decreases in size as well, making sensitivity an increased priority for bare wafer inspection — on the frontside and backside, at the edge and in the notch.

With an eye on evolving requirements for advanced node bare wafers, manufacturers are seeking inspection solutions with automatic defect classification (ADC) capabilities to perform outgoing quality assurance for wafers, including polished wafers and those with silicon epitaxial layers. Armed with these ADC capabilities, customers can significantly reduce the need for time-consuming and costly manual review.

The frontside, bulk, backside, edge and notch — each of these areas needs to be inspected to ensure the quality of the silicon wafer and the successful fabrication of advanced devices on the wafer. We'll start with frontside and bulk before moving onto backside, edge and notch inspection, the main focus of this blog.

Frontside and Bulk

For bare wafer inspection, wafer-makers are interested in detecting many of the same defects that affect wafer quality in other process steps: particles, scratches and pits. Additionally, manufacturers are also particularly interested in identifying pinholes and air pockets that are found in the bulk. There is a keen interest in not only detecting these voids but also determining their depth as it might affect the criticality of such defects. This is because any void near the bottom of the wafer will most likely not affect device characteristics since the wafer backside is typically ground down after the device is built.

Air pockets are created during the monocrystalline pulling step. Air trapped between the polysilicon chunks in the crucible is released into the melt as gas bubbles, which are then incorporated into the crystal as air pockets. Once the monocrystalline ingot is ground down to a desired diameter, it is then sliced to form the wafers. Air pockets that intersect

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the top or bottom of the wafer end up forming pits on the wafer surface, which may need to be distinguished from particles.

Brightfield reflectometry, darkfield reflectometry and laser scatterometry are typically used to identify and flag frontside surface defects like scratches, particles, and pits, while an infrared-based technique is required to penetrate through the bulk silicon in order to identify air pocket defects.

Backside

Backside defects —like particles — impact the rest of the wafer. For example, a defect on the backside can lead to wafer flatness, which, in turn influences depth of focus and image placement in the extreme ultraviolet (EUV) lithography process. To meet the demands of EUV lithography, these leading-edge epi-deposited substrates have tighter specifications than previous substrates. Consider 3-5nm logic nodes: the image placement requirement can be as low as 3nm, according to the August 2022 Semiconductor Engineering article, "How Overlay Keeps Pace with EUV Patterning." As a result, requirements for advanced nodes are stringent.

Hotspots are another matter of concern for backside defect detection because these particles can impact electrostatic chucking, which is utilized in various process steps like etch or implant. Backside particles can create localized hotspots which may impact process non-uniformity if that process is sensitive to substrate temperature. In extreme cases, backside particles can also cause wafer breakage as the wafer is pulled flat on an electrostatic chuck.

Finally, these particles may impact more than just the backside — they can also fall off the backside and land on the frontside of a subsequent wafer while in transport or in the front-opening unified pod (FOUP), opening the door to possible killer defects.

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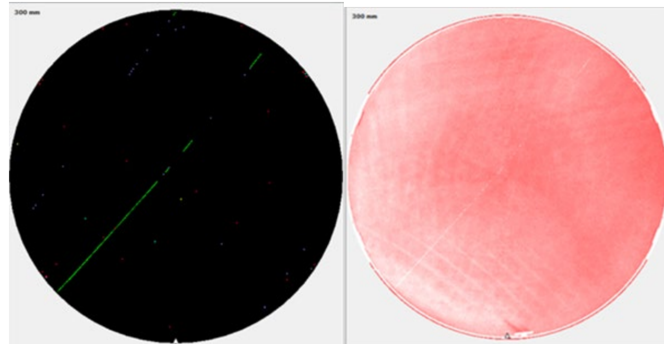

Figure 1: Backside defect map (left) and backside haze map (right).

Edge and Notch

An edge inspection tool should examine the wafer for particles, scratches, chips and cracks on the entire bevel region. Polishing- or handling-related chips or cracks can result in a high stress point on the pristine crystalline structure. When the wafer undergoes thermal processes, these defects can create significant stress buildup. Such stress can break the crystalline wafer, causing catastrophic wafer breakage during which pieces fall on other wafers or sensitive tool surfaces like chucks and robot end-effectors, leading to contamination and significant process tool downtime.

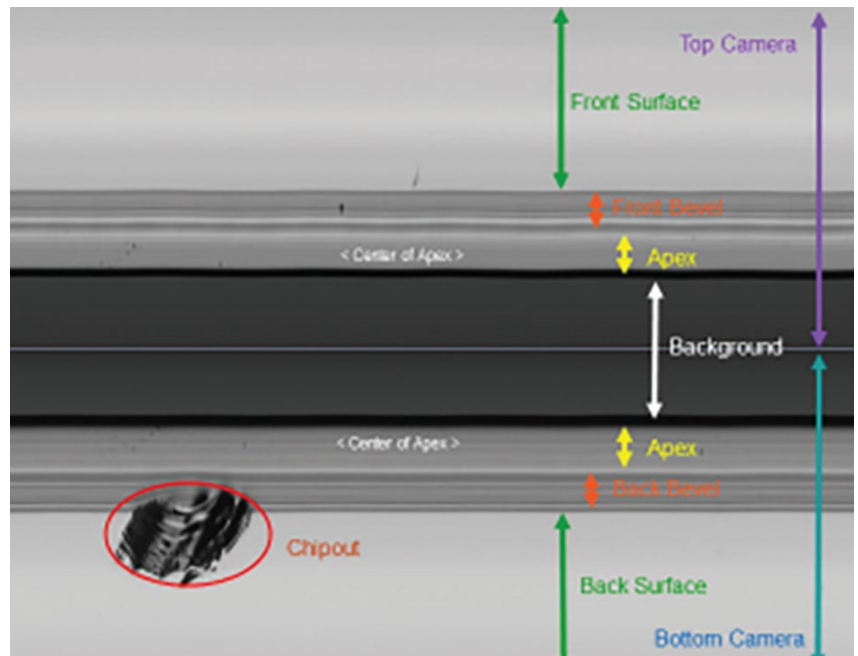

Figure 2: Edge image, chipout defect in Zone 4 and 5.

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As the part of the wafer denoting the orientation of crystal growth, the notch should be inspected for orientation and many of the same defects that plague the backside and edge, like particles, cracks and scratches. The requirements to control such defects on both edge and notch are becoming increasingly stringent as the potential impact to yield later on in the device manufacturing processes becomes high.

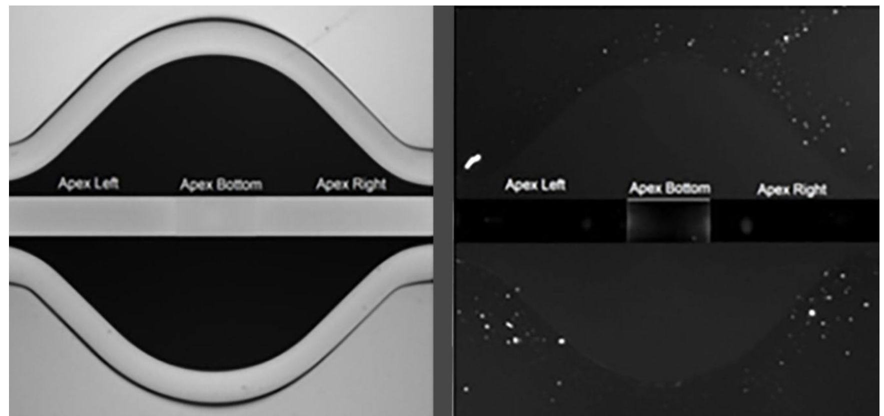

Figure 3: Notch brightfield image (left), notch darkfield image (right).

Conclusion

Due to the stringent requirements of bare wafers for the advanced node market, manufacturers are looking for tools with increased sensitivity and solutions with increased throughput and lower cost of ownership. Whether the task at hand involves backside, edge or notch, new inspection technologies can help manufacturers solve the Case of the Killer Defect and deliver results that are far from elementary.

About the author

Burhan Ali is product marketing manager, inspection products, at Onto Innovation.