innovation®
onto

3D NAND needs 3D metrology

By: Nick Keller and Andy Antonelli,
Onto Innovation

Content as published on
Semiconductor Engineering blog post, August 2023.

You've read the reports: the memory market is floundering as the semiconductor industry moves through another scarcity/surplus cycle.

Be that as it may, innovation is happening as the industry continues to pursue increasingly higher three-dimensional stacks, with 3D NAND stacks taller than 200 layers entering production.

However, there are challenges. Among those: conventional optical critical dimension (OCD) metrology systems have difficultly measuring the tungsten (W) recess in the wordline (WL) slit following the replacement gate step. This is particularly a problem as high-aspect ratio (HAR) stacks reach 96 layers or higher. For manufacturers, the ability to measure the W recess is critical. Under-etching the W replacement gates in the recess can cause wordlines to short, while over-etching the W gates can damage cells or cause a short from the wordline to the source line.

Presently, there is no in-line process control solution that can measure the W recess to the bottom of a 3D NAND device following the replacement gate process. Beyond just a few layers in the stack, the entire structure becomes opaque in the ultraviolet/visible/near-infrared region, the typical wavelengths of many OCD systems. Additionally, increased wordline slit pitch scaling further reduces the already minimal optical signal from the top of the 3D NAND structure to the bottom.

One such opportunity comes in the form of a non-destructive technique using the mid-infrared wavelength to measure the W recess in 3D NAND structures following the etching process. Mid-infrared (mid-IR) optical critical dimension (CD) metrology (or IRCD) has been used to measure channel hole etch and amorphous-carbon hard mask etch, but we've found that it can also be used to measure the W recess all the way to the bottom of a 3D NAND device following etching and the replacement gate process, thanks to a novel technique involving surface plasmon polaritons and a specialized via to periphery (VtP) target.

innovation®
onto

3D NAND needs 3D metrology

By: Nick Keller and Andy Antonelli,
Onto Innovation

Content as published on
Semiconductor Engineering blog post, August 2023.

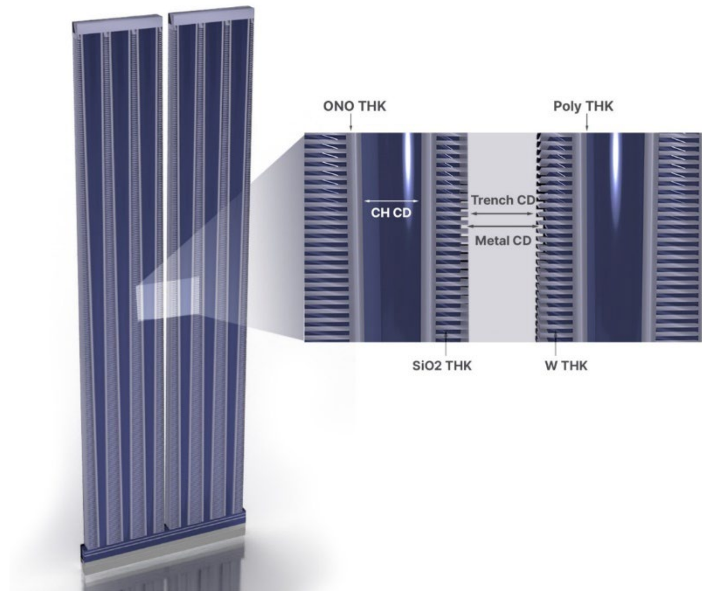

Figure 1. Large W vias replace the channel holes in the 3D NAND device in a specialized via to periphery (VtP) target.

The VtP Target

Using a finite-difference time-domain (FDTD) and OCD simulations, a specialized measurement target was developed that enables mid-IR light to penetrate through metal and silicon dioxide pairs to reach the bottom of the W recess and, in turn, allow for the measurement of the Z-profile of the W recess in the wordline slit.

With the VtP structure, light can couple to surface plasmon polaritons (SPPs), which are collective longitudinal oscillations of electrons in plasma, and propagate through the wordline recess and SiO_2 liners to the bottom poly-Si layer of the 3D NAND device at wavelengths of 5, 6, 7 and 10µm. At wavelengths of 8 and 9µm, the absorption properties of SiO_2 impact this ability to see through the structure, largely due to the strong Si-O bond, causing the real part of the dielectric function to become negative, so that SPPs cannot be excited. However, SPP oscillations in the wordline slit are visible at wavelengths of 6, 7 and 10µm, and SPP oscillations are also apparent in the SiO_2 liner surrounding the W vias at a shorter wavelength compared to the slit region due to the smaller gap distance. More importantly, this VtP/SPP technique works on HAR structures at 200 layers and higher.

innovation
onto

3D NAND needs 3D metrology

By: Nick Keller and Andy Antonelli,
Onto Innovation

Content as published on
Semiconductor Engineering blog post, August 2023.

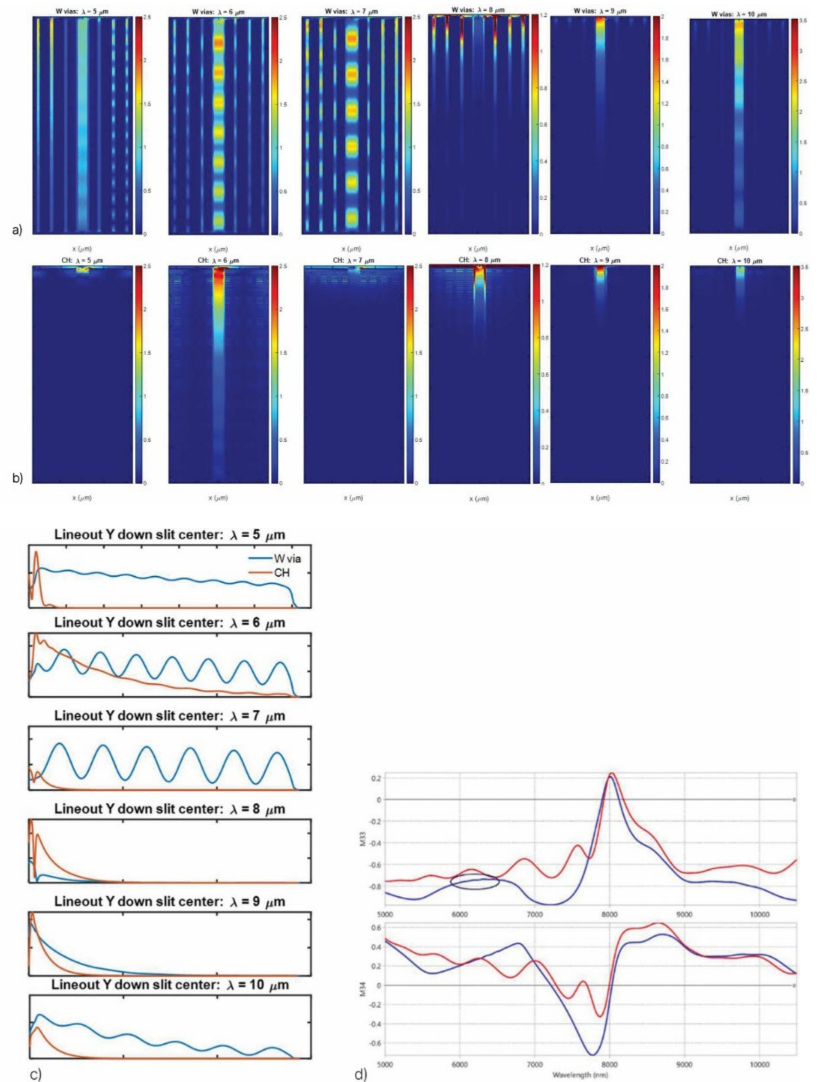

Figure 2: FDTD simulations offer an accurate physical model of how SPPs propagate in the structures, with the electric field propagating to the bottom of the device structure at a wavelength of 6µm (shown in Figure 2b and 2c), and it corresponds to highly attenuated oscillations in the simulated spectra from wavelengths of 6 to 6.5µm (circled in Figure 2d).

CONCLUSION

The W recess step is a key part of the 3D NAND manufacturing process. But by using a VtP structure, an IRCD metrology system designed for 3D NAND and HAR devices, and model-guided machine learning, this important challenge can be overcome. This technique demonstrates the ability to measure and capture CD/recess profile variation for the entire W recess in HAR devices of 200 or more layers, providing a novel metrology solution for the next generation of 3D NAND devices.

3D NAND needs 3D metrology

By: Nick Keller and Andy Antonelli,
Onto Innovation

Content as published on
Semiconductor Engineering blog post, August 2023.

About the author

Nick Keller is an applications director at Onto Innovation.
Andy Antonelli is a senior director and fellow, advanced research and development, at Onto Innovation.