The great lithography debate: Copper clad laminate or glass substrates?

By Doug Brown [Onto Innovation]

For many in the semiconductor industry, the future is clear. Glass substrates are destined to play an important role in advanced packaging. Compared to organic substrates, glass offers better thermal management, enhanced electrical properties, new form factor possibilities and improved conductor routing. All of which make glass substrates an innovative advanced packaging option for artificial intelligence (AI) and high-performance computing (HPC).

One thing is certain—the glass substrate future is poised to arrive later than originally expected. Previously, many in the industry thought that the transition from copper clad laminate (CCL) substrates to glass substrates would occur when redistribution layers (RDLs) shrank below 5/5µm line/space (l/s). But with today's equipment and processing solutions, the life of CCL in substrates may be extended beyond the 5/5µm l/s demarcation point and reach 2/2µm l/s.

Whether or not manufacturers should use substrates with CCL (**Figure 1**) or glass substrates is likely to be the subject of debate for years to come. In fact, the argument may only be resolved when one substrate, either those with CCL or made from glass, reaches the 2/2µm l/s finish line first—and does so while offering more reliability and lower cost. Until then, let's explore the pros and cons of CCL and glass substrates.

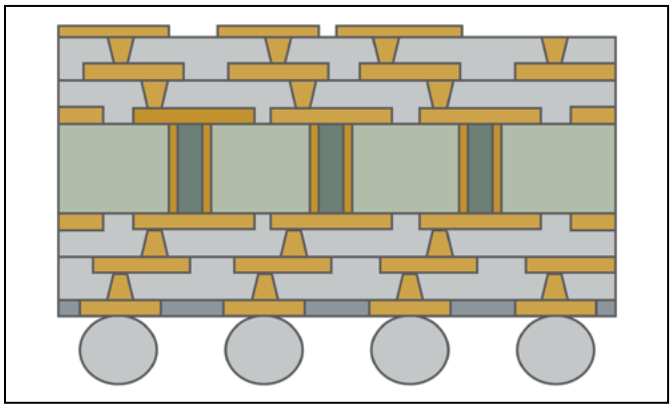

Figure 1: Copper clad laminate substrate.

The CCL argument

With most advanced IC substrates (AICS) currently using CCL and Ajinomoto build-up film (ABF), there is significant industry momentum to propel CCL technology to its full potential of 2/2µm l/s. After all, CCL has some significant advantages for AICS. For one, CCL's properties and limitations are well understood. Two, CCL is robust and nearly indestructible. But pushing AICS with CCL beyond the current RDL line/space requirements and overlay limits will require process innovation and additional lithography steps. For instance, laser-drilled vias in ABF will not support the less than 10µm via dimension requirements needed for state-of-the-art advanced packages with RDLs of 2/2µm l/s. The alternative process will be either photo-imageable dielectrics (PID) or ABF with a lithography patterned hardmask.

The benefits of using lithography for both RDL and via layers are significant. Not only will the overlay between via layers and RDL be improved, the via dimension could easily be reduced to less than 5µm. And by using lithography to pattern both the via and RDL structures, it will be possible to shrink the design rules of the via to the RDL landing pad, which currently limits package design rules, resulting in low interconnect density and additional RDL layers. At the moment, the via to RDL landing pad dimensions for 9/12µm RDL are more than 50µm, with a contingency for overlay errors between the via and the pad of more than 10µm. If overlay were improved by utilizing lithography for both RDL and vias, these dimensions could shrink significantly. However, this process adjustment would require a few additional steps. Regardless, the benefits would reduce overall costs, improve yield and, most importantly, extend the CCL roadmap to 2/2µm l/s.

Another lithography challenge for the 2/2µm l/s goal involves photoresist. Currently, the majority of AICS CCL manufacturers use dry-film negative-tone photoresist. This photoresist is laminated to the substrate and works well with larger RDL structures. However, at the 2/2µm l/s RDL node, a positive tone material would provide better resolution and process latitude. At this time, most positive photoresist is liquid and will require slit coating, or spray coating, unless a dry-film laminated version can provide the same imaging performance.

The AICS glass argument

When AICS CCL manufacturers identified the instability of CCL substrates and RDL design rule limits with their existing processes, they singled out glass as an attractive alternative (**Figure 2**). As it stands, glass has several selling points over CCL. At the top: glass provides a flat and distortion-free surface on which to build RDL and micro vias. The benefit here is that it enables even smaller features to be defined.

Glass, however, comes with its own set of challenges. Number one, it is fragile. This is especially true when it comes to the large panel sizes being employed today (510mm x 515mm and 600mm x 600mm) in advanced packages. Another drawback: glass substrates are also very thin. In some cases, less than 100µm. Given the fragility and thinness of glass substrates, sophisticated handling equipment will be required to process glass substrates through the various process steps to reduce the risk of breakage.

From a lithography perspective, a number of issues encountered with CCL can be immediately resolved by opting for glass

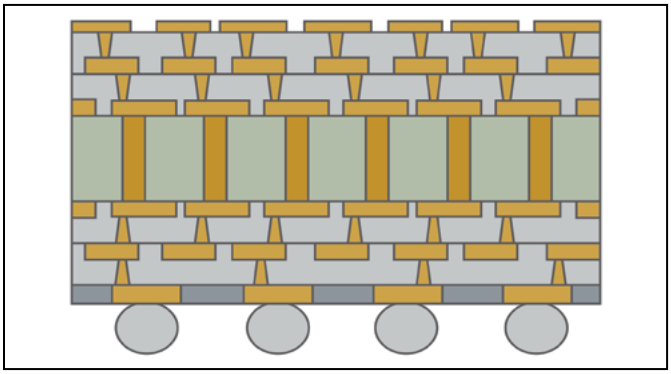

Figure 2: Glass substrate.

substrates instead. For instance, overlay of the via to RDL would be significantly improved as the glass would maintain its dimensions and not suffer from distortions by curing organic dielectric materials. The glass substrate would support higher resolution lithography. As such, the depth of focus budget would not be lost to substrate non-flatness. This would allow lithography tools to increase their numerical aperture (NA) to achieve the highly sought after 2/2µm l/s but sacrificing depth of focus (DOF) in the process, as described by Rayleigh's criterion. The reduced DOF, which continues to decline as resolution increases, would still be within a reasonable manufacturing DOF budget with glass substrates.

As with CCL, ABF, RDL and via processing would all need to be modified to meet 2/2µm l/s requirements. Some of the process steps described previously would be similar, but below 2/2µm l/s additional processes would need to be employed, especially for copper RDL plating seed removal. This particular process is isotropic and subjects the entire panel to a brief flash etch, which not only removes the seed material, but also the RDL metal, thereby reducing line width and impacting critical dimension (CD) uniformity. To resolve this issue, damascene processing has been proposed; this would require lithography to pattern RDL trenches in the ABF or PID and chemical mechanical planarization (CMP) to remove the excess copper to generate copper RDL interconnects.

Lithography system solutions

Currently, AICS CCL manufacturers are using extremely large field steppers (250mm x 250mm) with substrate formats of 510mm x 515mm and 600mm x 600mm. However, there is some discussion of 650mm x 650mm substrates, but these are not mainstream. These extremely large field steppers achieve high throughputs in excess of 110 panels per hour (PPH).

In addition to steppers, printed circuit board (PCB) manufacturers are experienced with laser direct imaging (LDI)

systems; as such, these lithography tools are also being used for RDL patterning involving AICS CCL. Of course, LDI has the advantage of not requiring reticles, but it is limited in resolution and throughput and not suitable for high-volume manufacturing (HVM). LDI is more of a research and development (R&D) tool to test out new designs and prototype larger geometry packages.

For AICS CCL processes, HVM steppers have low NA, which provide a large DOF; this allows steppers to easily accommodate the non-flatness of the substrate material. Currently, the RDL l/s resolution for extremely large field size HVM steppers is limited to 3µm. However, as we move closer to RDL of 2/2µm l/s, stepper solutions are available, albeit with smaller field sizes. The downside here is that such solutions limit package sizes to less than 60mm x 60mm—smaller than what most advanced packages will need—until the next generation of extremely large field steppers arrive with higher NA to support less than 2/2µm l/s.

At this time, R&D programs using CCL and/or glass substrates are racing toward the 2/2µm l/s node. HVM is still at 9/12µm l/s and is moving slowly towards 5/5µm l/s, with lithography requirements easily satisfied by the extremely large field size steppers. The HVM of glass substrates and 2/2µm l/s are not expected to occur until the end of the decade, so there is still time to gain a comprehensive understanding of the lithography requirements for 2/2µm l/s. Still, there are many lithography questions that need to be answered. For instance, what is the correct NA and DOF requirement and field size? Of course, customers are looking for these performance parameters to go beyond the laws of physics, so there needs to be more discussions and collaboration to determine what will be required.

In the past, the semiconductor industry referenced the International Technology Roadmap for Semiconductors (ITRS) to align original equipment manufacturers (OEMs) with material and substrate suppliers to deliver solutions with a clear indication of timing. Unfortunately, the Heterogeneous Integration Roadmap (HIR) does not have the level of detail required for lithography.

In the absence of a detailed industry-defined lithography roadmap, collaboration between OEMs and the material/substrate supply chain will be imperative. To help meet these challenges, Onto Innovation has established the Packaging Application Center of Excellence (PACE) in our Wilmington, Massachusetts, headquarters to address this issue. Collaborators are already engaged with the company in defining projects to help answer many of the most pressing lithography questions.

PACE will provide access to next-generation extremely large-field steppers, inspection, metrology and software capabilities that are currently in development. Furthermore, OEMs and supply chain partners will be able to develop next-generation materials using the center's infrastructure and its team's advanced packaging knowledge to provide customers with the solutions they need to accelerate their technology roadmaps, whether the future is in CCL or glass.

This collaborative opportunity posed by PACE may help determine the answer to the bigger question of which technology will win the race: copper clad laminate or glass. Until then, the debate continues.

Biography

Doug Brown is Senior Director of Product Management, Lithography, at Onto Innovation, Wilmington, MA. He is a graduate of the U. of Arizona, with a PhD in Electrical Engineering and a Master's in Electrical Engineering and another Master's in Physics. For the past 25 years, his focus has been on capital equipment development for the semiconductor industry, with tool introductions spanning plasma etch, deposition, ion implantation, liquid metrology and lithography. Email Doug.Brown@ontoinnovation.com