

The Specialty Device Surge Part 3: Solving the Process Control Challenges of MEMS, Photonics, Co-Packaged Optics, and More

By Christopher Haire,
Onto Innovation

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Every day, consumers rely on an invisible network of specialty semiconductor devices without realizing it. The smartphone in your pocket is a good place to start. It knows when you rotate the screen thanks to MEMS sensors, and its camera delivers crisp images through advanced CMOS image sensors. Meanwhile, fast charging technology, wireless connectivity, facial recognition, and high-frequency communications all depend on specialty power devices, radio frequency (RF) filters, and photonic technologies working seamlessly behind the scenes.

However, success in every specialty device category hinges on advanced process control solutions capable of ensuring what matters most is tightly understood and controlled. This may be shape, thickness, uniformity, defects, or material properties. And it all must be done at low cost of ownership while maintaining the throughput needed for high-volume manufacturing (HVM). For device manufacturers, failure to meet requirements doesn't just increase process complexity, it directly translates into longer ramps, missed customer commitments, and higher cost per device.

As we explored in the first two parts of this of our Specialty Surge series, these unsung heroes of modern electronics are rapidly scaling in complexity and volume, causing headaches for device manufacturers. In this final blog, we'll turn our attention to the strategies manufacturers can employ to make that pain go away. From advanced metrology to inspection and data-rich feedback for process control, we'll explore the capabilities enabling specialty devices to deliver the performance consumers expect at the scale manufacturers want.

Challenges Revisited

Before we go any further, let's recap the challenges specialty device manufacturers face, separated by device type. We'll begin with microelectromechanical systems, a.k.a. MEMS.

MEMS - MEMS include a variety of device types, including pressure sensors, gyroscopes, accelerometers, microphones, and surface acoustic wave (SAW)/bulk acoustic wave (BAW) radio frequency MEMS. These devices demand extremely tight control over specialized materials and fabrication steps, where small variations in film thickness, crystal orientation, and etch quality can directly degrade performance. Across MEMS, the core challenge involves maintaining wafer-level uniformity and precise feature profiles at scale to ensure consistent electrical, mechanical, and frequency behavior.

CMOS Image Sensors (CIS) - Modern CMOS image sensors are extremely sensitive to nanoscale process variation. As such, they require tight control of epitaxial thickness, dopant uniformity, and

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trench dimensions to achieve low noise and high light-capture efficiency. The challenge is amplified by the device's stacked architecture, which demands precise metrology and inspection across pixels, CMOS circuitry, and microlens layers to maintain uniform performance.

SiC and GaN Power Devices – SiC and GaN power devices face growing manufacturing challenges with the use of 300mm wafers. These challenges include crystalline defects, epi thickness variation, CD control, and backside and particle defects, all of which can impact yield and reliability. The core challenge for manufacturers of power devices is to maintain rigorous inspection and metrology for thick, defect-prone wafers while keeping cost-of-ownership competitive with conventional silicon power devices. The inability to distinguish benign defects from true killer defects early in the process can result in unnecessary scrap, escaped reliability failures, or overly conservative screening that limits output.

Photonics and Co-Packaged Optics (CPO) - Silicon photonics and co-packaged optics face significant manufacturing challenges due to the tight integration of lasers, waveguides, microlenses, and opto-electronic components within a single high-density module. Achieving reliable performance requires precise control of optical features, material uniformity, and multi-die assembly across multiple process domains where small variations can cascade into system-level loss.

Enabling Precision and Control in Specialty Device Manufacturing

Many of the challenges manufacturers face in the specialty segment can be addressed through capabilities integrated directly into the process flow. These capabilities enable real time adjustment and control of the fabrication process to maximize yields and improve device performance.

MEMS Devices - In RF BAW manufacturing, device performance is extremely sensitive to small variations in piezoelectric film thickness and acoustic stack uniformity. Traditionally, inline measurements help identify non-uniformity, but they do little to directly correct it. By combining high-precision, inline thickness metrology with software-driven run-to-run process control, manufacturers can move beyond passive monitoring to active performance control.

In this application, wafer-level thickness data are analyzed in real time to quantify across-wafer non-uniformity trends. That information is then fed directly into a downstream trimming process, where correction parameters are automatically adjusted on a wafer-by-wafer basis. The result is a closed-loop workflow that not only detects variation but actively compensates for it, reducing across-wafer non-uniformity by an order of magnitude. This integrated

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approach enables manufacturers to hit tight frequency specifications earlier in ramp, reduce binning losses, and improve RF BAW yield at production scale.

While this approach is specific to RF BAW devices, similar combinations of inline metrology and software-driven process control can be applied across other MEMS devices to stabilize critical dimensions, structural layer thickness, and structural symmetry that directly impact sensitivity, bias stability, and long-term reliability.

CMOS Image Sensors (CIS) - Modern CIS are built on stacked architectures that combine pixel structures, CMOS circuitry, and optical elements such as microlenses. While individual inspection or metrology steps can highlight issues within a single layer, many yield and performance problems emerge only when variability compounds across the full stack.

To address this, manufacturers increasingly correlate inspection and metrology data across multiple layers of the CIS flow. Structural and defect inspection of isolation trenches, metrology of epitaxial thickness and dopant uniformity, and optical-layer inspection are combined through software to build a unified view of pixel formation. This cross-layer correlation allows engineers to trace image non-uniformity or noise back to its true origin, whether it begins in epitaxy, implantation, trench definition, or optical layers, rather than discovering the issue late in the flow. By unlocking this multi-layer insight, manufacturers can intervene earlier, preserve image quality, and protect yield across increasingly dense pixel arrays.

SiC and GaN Power Devices – Wide-bandgap power devices such as SiC and GaN introduce a unique challenge: crystalline defects originating in the substrate can propagate vertically through epitaxial layers, becoming latent or killer defects in finished devices. Identifying which defects truly matter requires more than isolated inspection. It demands full wafer visibility and data correlation across process steps.

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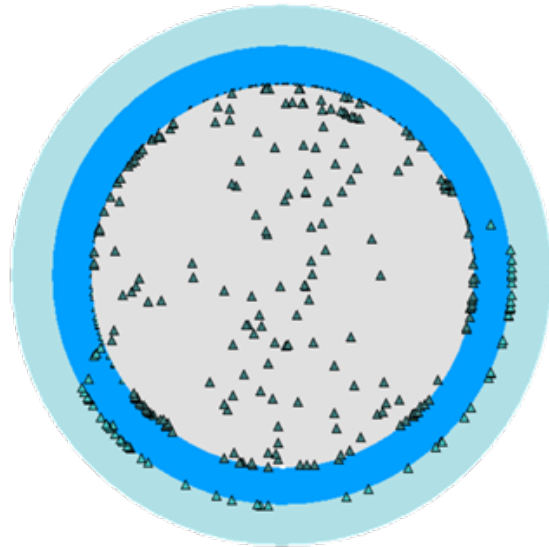


Figure 1: 360° full wafer defect view including sub-surface defects. In this image, concentric circular fields represent the frontside, edge and bevel areas of the wafer.

In this application, manufacturers begin by capturing a 360-degree view of the wafer, inspecting the frontside, backside, and edges to fully characterize the defect population. Substrate inspection performed before epitaxial growth identifies crystal defects early, while post-epi inspection reveals which of those defects persist and propagate into active layers. Software then correlates defect maps across both stages to isolate defects that originate in the substrate and extend through the epitaxial stack.

To further distinguish benign defects from true killers, electrical characterization is applied at the substrate level to measure defect resistivity. Defects that both propagate vertically and exhibit low resistivity—an indication of a high likelihood of current leakage or shorting under operating conditions—are flagged as true killer defects. This multi-modal, correlated workflow transforms inspection from simple defect counting into root-cause analysis, enabling smarter screening decisions, higher yield, and improved long-term device reliability.

Photonics and Co-Packaged Optics (CPO) - Photonics and co-packaged optics (CPO) represent one of the most integration-dense manufacturing environments where independently fabricated components must ultimately function together as a single optical system. Defects that appear manageable at the component level can compound during assembly, leading to significant system-level optical loss.

At the component level, precision metrology and inspection are applied to each critical element. V-groove structures are measured

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for angle, depth, and height while simultaneously being inspected for particles or obstructions that compromise fiber alignment. Waveguides are analyzed for width, height, sidewall angle, and roughness, allowing manufacturers to correlate structural variation and local defects directly to optical loss. Microlenses are screened for deformation, cracks, or surface contamination that could degrade beam quality. Laser devices are monitored for mesa geometry and aperture dimensions, with feedback applied to etch processes, thereby stabilizing optical power and wavelength.

The challenge intensifies during final CPO assembly where multiple die are bonded, stacked, and aligned within a single module. Inspection at this stage must verify placement accuracy, bonding quality, and die planarity. Even minor warpage or misalignment can negate upstream process control. By integrating data from component-level inspection through final assembly, manufacturers gain visibility into compounding defect mechanisms and can intervene before system-level failures occur. In CPO manufacturing, this integrated approach is essential to protecting yield and optical performance.

Integrated Intelligence

Across MEMS, CIS, power, and photonic devices, specialty device manufacturers may find that the greatest value comes from integrating metrology and inspection data across tools, layers, and process steps. By correlating structural, optical, electrical, and defect information—often with 360-degree wafer visibility—manufacturers can move from reactive defect detection to proactive process control.

This integrated approach is critical to achieving the performance, yield, and reliability required for today's most advanced and highly specialized semiconductor devices. Ultimately, manufacturers benefit most when inspection and metrology stop being isolated checkpoints and instead function as an integrated manufacturing intelligence layer that shortens ramp times, protects yield, and accelerates time to market. The challenge is no longer whether defects can be found, but whether insight can be gained early enough to act before yield, schedule, or reliability are impacted.

Biography

Christopher Haire is a marketing content specialist at Onto Innovation and a former business journalist.