Yield Prediction Technology A Game Changer for Cutting Costs and Reducing Ramp Time in FOPLP Lithography

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***Abstract*— Fan-out panel-level packaging (FOPLP) offers significant advantages in meeting the aggressive demands of AI chips, particularly by supporting larger package sizes and optimizing substrate utilization. However, as the AI market continues to expand rapidly, the challenge lies in how to swiftly transition to mass production. A second challenge is yield; AI chips integrate multiple control units and high-bandwidth memory (HBM) during the packaging process. These components are expensive. Therefore, maximizing yield at every step and identifying defects early to minimize losses is critical. Yield prediction technology addresses both the speed and yield challenges of FOPLP lithography. This approach utilizes an offline metrology tool to measure die shifts or pattern distortions on the panel substrate. The metrology data is then analyzed using machine learning algorithms, which, when combined with customized process parameters, can accurately predict overlay errors and overlay yield. This predictive insight allows for more informed decision-making and earlier intervention in the lithography process. In this study, we will detail how yield prediction technology functions and how its application in the early R&D stages can accelerate development. We will also discuss how yield prediction technology can be implemented in mass production lines for pre-emptive quality control. With the expected significant growth of FOPLP over the coming years, we believe that yield prediction technology will provide a clear path toward achieving both rapid production and high yields in FOPLP lithography.**

Keywords*— *Advanced packaging, Chiplet, 2.5D packaging, Fan-out Panel-level Packaging (FOPLP), Lithography, Overlay, Yield Prediction, Lithography Optimization, Ramp Time, Rapid, Yield.

I. Introduction

Artificial intelligence (AI) is projected to grow at an impressive compound annual growth rate of 15% to 40% from 2023 to 2030 (Fig. 1) [8]. This rapid growth is driven by increasing demand for high-performance computing and substantial data transfer requirements. To meet these challenges, heterogeneous integration has emerged as a pivotal solution, offering significant benefits in terms of cost efficiency, performance enhancement, and power consumption reduction. One notable example is AMD's Ryzen 7000 series processors, which leverage a heterogeneous design. The high-performance computing cores are manufactured using an advanced 7nm process, while the I/O modules utilize a 12nm process. This approach achieves a cost reduction of approximately 40% without compromising performance. These advancements highlight the transformative potential of heterogeneous integration in AI and semiconductor technologies. As AI applications demand ever-increasing computational power, the need for integrating more high bandwidth memory (HBM) and high-performance chips within a single package has grown exponentially. Consequently, the physical size of semiconductor packages has expanded significantly. Fig. 2 illustrates the steady increase in packaging size from 2021 to 2024, underscoring the industry's response to these requirements.

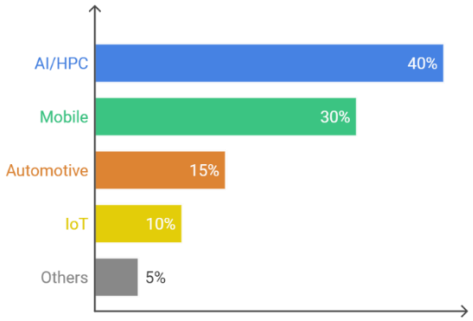


Fig 1. Semiconductor Marketing Sharing Prediction. From the 2024 IEEE International Solid-State Circuits Conference (ISSCC), a forecast of the semiconductor market's platform-based distribution in 2030 was presented, with the total market value estimated to reach $1 trillion.

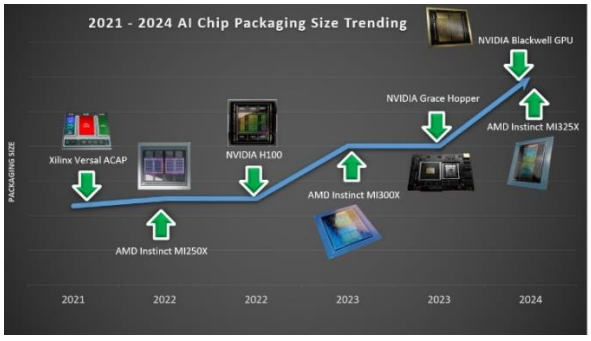


Fig. 2. AI Chip Packaging Size Trends. This Fig. illustrates the year-on-year growth in chip dimensions, highlighting the increasing demand for larger packaging to accommodate advanced integration requirements.

As packaging sizes continue to grow, substrate utilization has become a critical issue [5]. In this context, fan-out panel-level packaging (FOPLP) is regarded as one of the best solutions to address this challenge. FOPLP not only offers high substrate utilization but also achieves high throughput and significant cost reduction. As shown in Fig. 2, FOPLP demonstrates clear advantages in substrate utilization and output compared to traditional wafer-level packaging. For instance, a 300mm wafer achieves only about 55% substrate utilization, with an average output of six units per wafer. In contrast, FOPLP using panel substrates can achieve a substrate utilization rate ranging from 74% to 86%, with an output of 12 to 30 units per panel. This improvement is due to the larger effective area of panel substrates and the more efficient management of idle regions during processing, thereby enhancing material utilization and cost efficiency. Moreover, the advantages of FOPLP in substrate utilization extend beyond higher production efficiency. They also contribute to reduced waste in the manufacturing process. This is particularly significant for the development and mass adoption of next-generation advanced packaging technologies, especially in applications such as AI chips and high-performance computing (HPC).

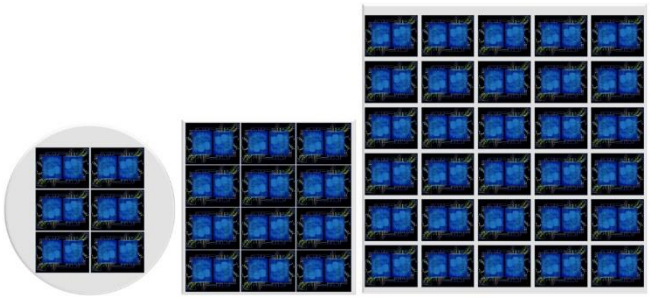


Fig 3. Comparison of Substrate Utilization Efficiency. 300mm wafer utilization: 55%, 6 units a substrate. 300mm panel utilization: 86%, 12 units a substrate. 510 x 515mm panel utilization: 74%, 30 units a substrate.

Yield prediction technology represents a breakthrough innovation, providing significant solutions to key challenges in FOPLP lithography. This advanced technology plays a critical role in early stage yield control, helping to minimize rework rates and offering a reliable tool for early stage yield prediction. By leveraging detailed analysis of various device and process conditions, yield prediction technology effectively reduces R&D cycles, enabling faster time to market. In this study, we delve into the specific challenges associated with FOPLP lithography, including complexities in defect management and achieving consistent yield during mass production. We further demonstrate yield prediction technology, detailing its methodologies, algorithms, and integration into the manufacturing workflow. By utilizing predictive analytics and machine learning models, yield prediction technology not only identifies potential in-line process defects but also recommends actionable solutions to optimize production parameters at an early stage, enabling a faster ramp-up.

II. Experiment Details

A. *FOPLP Lithography Challenge and Correction Strategies Analysis*

Pattern errors and die shifting are among the major challenges in FOPLP lithography. These errors must be addressed during the lithography process; otherwise, they can result in overlay shifting, ultimately degrading overlay yield. Such issues typically originate during the reconstitution and redistribution layer (RDL) build-up processes. Fig. 4 illustrates the regular error distribution observed on a 510 x 515mm FOPLP substrate. In the heat map, blue regions represent negative errors, while red regions denote positive errors [1]. Upon analyzing the heat map, it becomes evident that the error pattern transitions from negative to positive and back to negative across the substrate. In the adjacent Fig., the error distribution is shown to be highly region specific, further highlighting the non-uniformity. These observations reveal the presence of non-linear error patterns within the substrate, posing a significant challenge for achieving high overlay precision [7]. Addressing these non-linear errors is critical for the exposure tool used in FOPLP lithography to ensure process reliability and yield optimization.

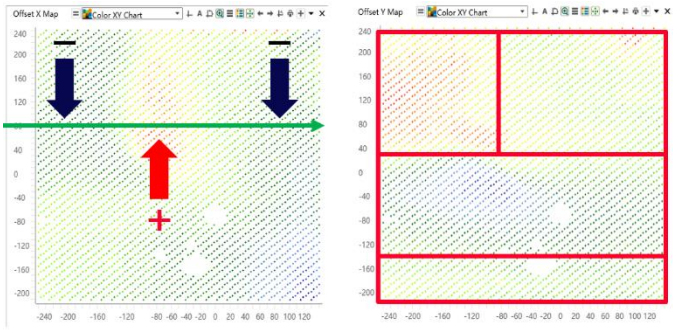


Fig 4. Heat maps of regular FOPLP substrates error distribution . Blue regions indicate negative errors, while red regions represent positive errors. The heat maps reveal non-linear pattern errors across the substrate.

To address non-linear errors in the lithography process, various correction strategies are evaluated, as shown in Fig. 5 [2][3]. Global correction, the most common method, applies a single adjustment for the whole substrate. While it achieves high throughput, it fails to address non-linear errors effectively, resulting in low yield [6]. Zone correction improves yield compared to global correction, with field data indicating yields between 40-80%, but it remains insufficient for optimal results. Die-by-die correction significantly enhances yield by aligning and exposing each die individually, but the throughput is extremely low due to the time-intensive nature of the process. To mitigate this, site correction has been introduced, allowing multiple dies to be processed in a single step. This approach balances yield improvement with enhanced throughput. Each correction method presents unique advantages and limitations.

Identifying an optimal balance between yield and throughput, termed the "sweet spot," is critical for efficient lithography operations in FOPLP.

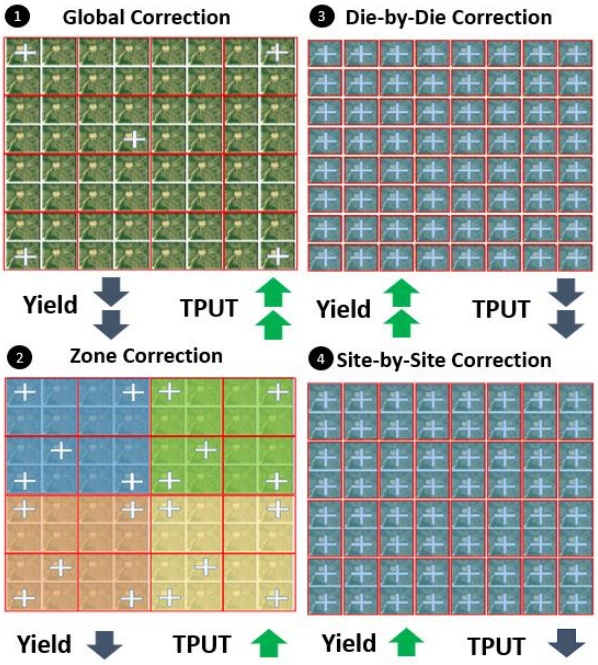


Fig. 5. Lithography correction strategies to address the non-linear errors. Global correction. A single correction is applied uniformly across the entire substrate. Zone correction. The substrate is divided into zones, and corrections are applied to each zone individually. Die-by-die correction. Each die on the substrate is aligned and corrected individually. Site-by-site correction. Corrections are applied to multiple dies within a larger exposure field at once.

B. Sweet Spot Between Overlay Yield and Throughput

Identifying the sweet spot in a lithography process involves balancing yield and throughput to achieve optimal performance [2][3]. Based on the analysis in the previous section, different correction strategies exhibit unique trade-offs. Global correction offers high throughput but low yield, while zone correction improves yield but reduces throughput. Die correction delivers the highest yield but suffers from extremely low throughput due to its time-intensive nature. Site correction balances these factors, improving throughput while maintaining good yield. To identify the sweet spot, process data is plotted to visualize the trade-offs between yield and throughput. By defining an acceptable yield threshold represented, for instance, by a green line on the chart, two intersection points are revealed. The point with the higher throughput is considered the sweet spot for the process, shown as Fig. 6. However, this method requires significant time and effort, as adjustments often necessitate repeated trials and data re-analysis. Achieving a quick, accurate, and reliable identification of the sweet spot remains a significant challenge in FOPLP lithography.

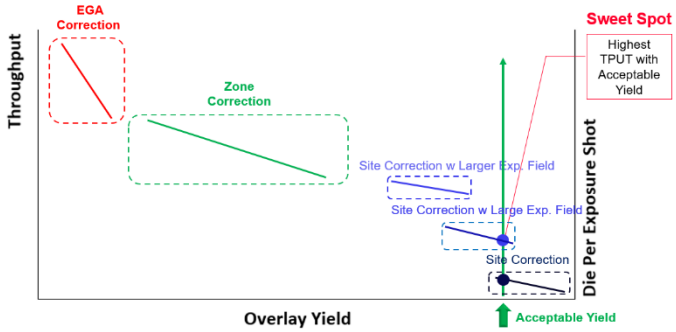


Fig. 6. Performance analysis and “sweet spot” identifying. Determining the sweet spot in a regular lithography process requires significant time and effort, as adjustments often necessitate repeated trials and data re-analysis.

C. Yield Prediction Technology

Yield prediction technology utilizes an offline metrology tool to capture data on pattern errors and die shifting across substrates, a process known as mapping. The yield prediction algorithms analyze this mapping data in conjunction with critical parameters such as exposure fields, die layouts, panel layouts, overlay thresholds, and other relevant process variables to accurately forecast overlay yield [4]. These algorithms generate comprehensive visual tables and charts, enabling users to proactively identify and understand the underlying causes of yield loss. This advanced analysis facilitates the implementation of targeted yield improvement strategies. Fig. 7 illustrates the operational workflow of the yield prediction technology.

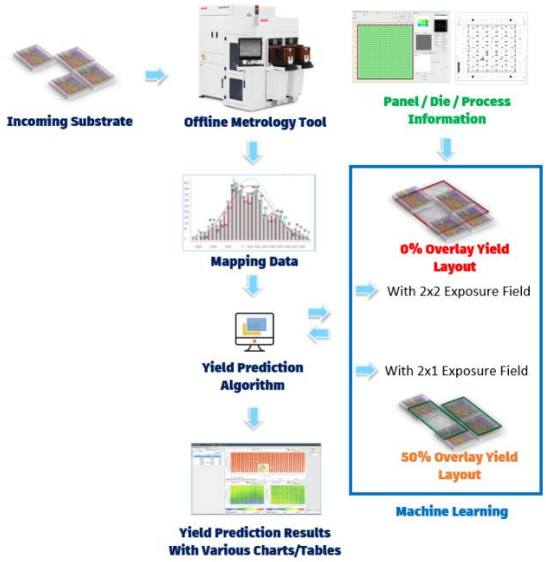


Fig. 7. Yield prediction technology working scenario. An offline metrology tool captures data from a substrate, creating a comprehensive mapping dataset. The algorithms analyze the mapping data to predict overlay yield. The results are presented through a variety of visual formats, including detailed tables and graphical charts, enabling intuitive analysis, and facilitating root cause identification.

D. Yield Prediction Technology Performance and Analysis

To demonstrate the capabilities of this yield prediction technology, it was integrated into a high-volume manufacturing process and validated using production substrates. Initially, the technology was employed to predict the yield of several substrates prior to completing the lithography process. Afterward, the final yield was measured using a third-party inspection tool, and the predicted yield was compared against the actual yield to evaluate the accuracy of the predictions. In the initial assessment, the yield prediction errors ranged between 1.2% and 2.7% (Fig. 8). While these results were promising, they were not deemed satisfactory.

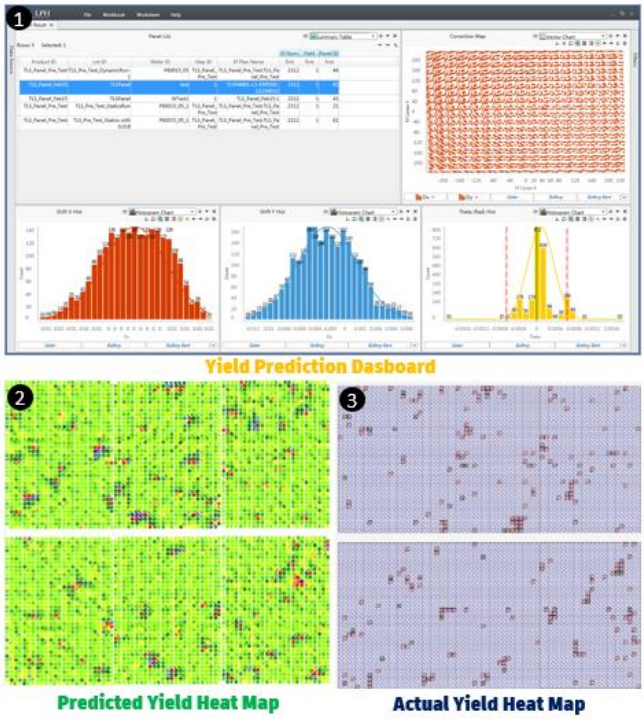


Fig. 8. Yield prediction demonstration. Yield prediction dashboard. Includes predicted yield number, vector map and histogram charts for various deviations. Predicted yield heat map. The green dots indicate good overlay while red and blue dots indicate overlay is out of threshold; the yield number is 97.45%. Actual yield heat map. The blue dots indicate good overlay while red dots indicate the overlay is out of threshold. the actual overlay number is 98.82%. A comparison between the predicted and actual values reveals a difference of 1.37%. The results were not deemed satisfactory compared to our expectations.

An investigation was conducted to identify the root causes of the discrepancies. It was found that the primary source of error arose during the inspection process where ambiguous patterns were escalated for manual judgment. Human variability in these judgments contributed significantly to the observed discrepancies (refer to Fig. 9).

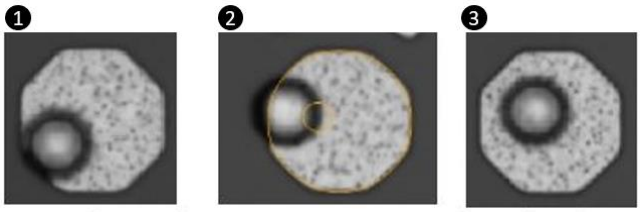


Fig. 9. Overlay image variations can impact final yield due to operator errors. VIA at PAD edge. VIA slight over PAD edge. Good overlay of VIA and PAD. The metrology tool struggled with ambiguous patterns (example: and), leading to manual judgment and variability induced discrepancies of yield number.

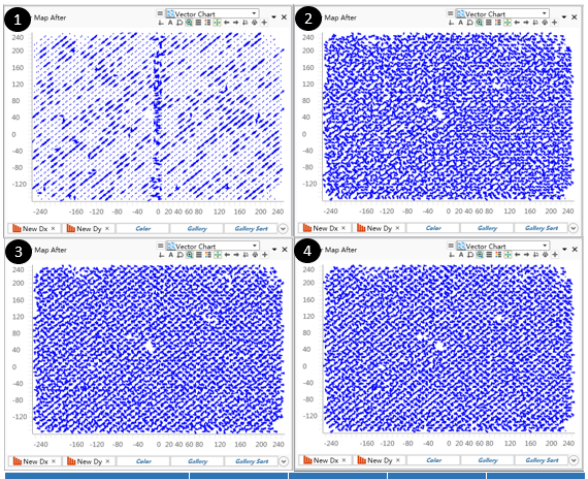
To address this issue, a comprehensive standardization and training program was implemented for inspection operators to minimize human-induced errors. The substrates were then re-evaluated, and the final yields were measured again. Following the improvements, the prediction errors were significantly reduced, achieving a range of 0.2% to 0.8%.

III. Analysis and Discussion

A. Discussion on Utilizing Yield Prediction Technology for Early Stage R&D

In the previous section, we highlighted the importance of identifying the sweet spot in FOPLP lithography to meet the demands of mass production. However, this process traditionally requires extensive time and effort, as it relies on repetitive experimentation under varying process conditions to build a comprehensive dataset. To accelerate this process, yield prediction technology offers a powerful solution by simulating final yield outcomes under different process parameters and conditions. By leveraging this technology, users can identify optimal parameters through simulations and then validate the predictions by running qualification substrates. This approach significantly reduces the time and cost associated with traditional trial-and-error methods during the R&D stage (Fig. 10).

Additionally, yield prediction technology generates various visualized charts and analytical tools, enabling users to preemptively identify potential substrate issues. These insights help pinpoint specific problems and guide corrective actions, streamlining process optimization and improving overall efficiency (Fig. 11).



Process Condtion	1	2	3	4
Predict Yield (%)	100%	99.89%	99.84%	99.57%

Fig. 10. Yield prediction results by using various process conditions. By leveraging this data-driven approach, users can accelerate process refinement, reduce trial-and-error iterations, and achieve more efficient improvements during the R&D stage, ultimately enhancing production efficiency and yield outcomes.

Fig. 11. Various visualized charts and analytical tools of yield prediction technology [4]. Various parameters for in-depth analysis. X-axis overlay error heat map. Y-axis overlay error heat map. A comparison of these maps reveals that the Y-axis exhibits the most significant overlay errors, which directly contribute to yield loss. This insight enables users to pinpoint the root cause of the issue and take corrective actions effectively, thereby improving overall process performance.

B. Discussion on Utilizing Yield Prediction Technology for Real-Time In-line Process Monitoring

This section discusses the application of yield prediction technology for real-time in-line process monitoring, enabling early defect detection. In a standard lithography workflow, a substrate must pass through multiple stages, including coating, exposure, development, and post treatment, before final inspection determines the overlay yield. Any errors occurring during these steps can result in rework or permanent yield loss. As discussed earlier, die shifting and pattern distortion are significant challenges in the FOPLP lithography process, both of which pose a high risk of inducing yield loss. To address these issues, implementing an early-stage defect detection system becomes critical. Such a system ensures timely identification of defects, safeguarding final yield and reducing the manpower, time, and costs associated with rework. By integrating real-time monitoring with yield prediction technology, manufacturers can enhance process reliability and production efficiency. Fig. 12 illustrates the implementation of yield prediction technology within a mass production process and its role in achieving early stage defect detection. The technology integrates seamlessly into the production workflow, enabling real-time monitoring and analysis to identify potential defects early in the process.

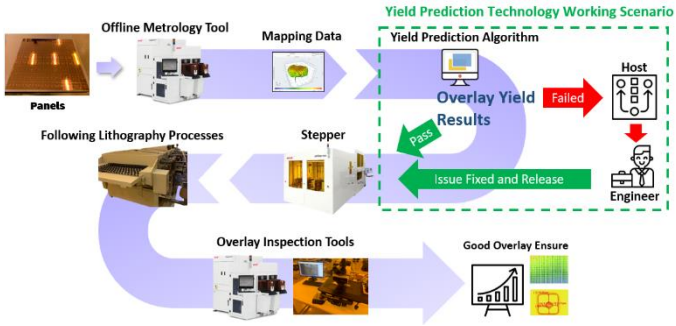


Fig. 12. The workflow of yield prediction technology for real-time, in-line process monitoring. By leveraging predictive insights, users can proactively address issues in early stage, ensuring higher yield outcomes while minimizing rework, downtime, and associated costs.

IV. Conclusion

This study delves into the challenges of FOPLP lithography, emphasizing the critical concept of the sweet spot — the optimal balance between yield and throughput. Identifying this balance in the R&D stage often demands significant resources, including time, manpower, and cost. To overcome these challenges, the study introduces yield prediction technology as a solution. The research highlights how yield prediction technology facilitates rapid production ramp-up and achieves substantial cost savings. Through case studies and empirical data, research demonstrates the technology's ability to streamline processes, improve manufacturing efficiency, and ensure higher yield rates. By providing actionable insights and predictive capabilities, this technology addresses key lithography challenges, such as die shifting and pattern distortion, which directly impact yield outcomes. Yield prediction technology represents a paradigm shift in FOPLP lithography. It not only resolves existing production challenges but also establishes new benchmarks for innovation, efficiency, and competitiveness in advanced packaging technologies, making it an indispensable tool for next-generation FOPLP lithography manufacturing technology.

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