

Overcoming FOPLP die placement error

By Keith Best [Onto Innovation]

It is well understood that advanced packaging applications require high performance, low cost, increased functionality and improved reliability that 2.5D and 3D packaging solutions provide. Fan-out panel-level packaging (FOPLP) is one of the technologies that has the potential to meet these packaging requirements. Similar to fan-out wafer-level packaging (FOWLP), FOPLP processes reconstitute die on a substrate, in this case a rectangular platform that can be significantly larger than the standard 300mm diameter wafer form. In the reconstitution process, die are displaced from their nominal grid locations during the epoxy molding compound process and sometimes during subsequent processing steps. This fan-out technology delivers more space for redistributed I/O connections, providing increased flexibility for homogeneous and heterogeneous integration. Importantly, the larger panel format can support more packages per substrate than the 300mm wafer form, and the final package size can be increased by adding space between the die.

Although FOPLP processing has many advantages, it also faces significant challenges. One critical challenge is die placement error, which occurs when die are positioned during the reconstitution and molding process. These placement errors are amplified with the larger panel format when compared to reconstituted wafers, and errors of 50 μ m or more are not unusual. In order to guarantee acceptable yield, these errors must be corrected during the lithography process using site-by-site corrections. Conducting metrology and site-by-site exposures on the lithography system is very time consuming. Substrate alignment and error correction may be calculated using global alignment, but this correction does not accommodate nonlinear die placement errors. It has become clear that only site-by-site corrections can deliver the overlay required to maintain good yield. Executing site-by-site alignments in the stepper reduces throughput and increases cost enough to make that approach to FOPLP processes impractical. A new approach uses an external metrology

tool to capture die placement error data from a panel and feeds that information forward. The “feed-forward” solution optimizes the stepper, site-by-site, for X, Y and rotation offsets, during exposure. Visualization of the metrology data allows the user to characterize upstream and downstream processes. Moreover, analytical capabilities predict yield as a function of exposure field size, thereby allowing the user to balance throughput against yield in real time. This solution can significantly increase stepper throughput, reduce cost and increase productivity while ensuring high yield.

Die placement challenges

Generating reconstituted panel substrates creates translational and rotational die placement errors. The “pick and place” process itself introduces initial errors that are exacerbated during the mold process, and by instability of the mold compound throughout repeated processing cycles. With redistribution layer (RDL) features currently achieving dimensions as small as 2 μ m, die

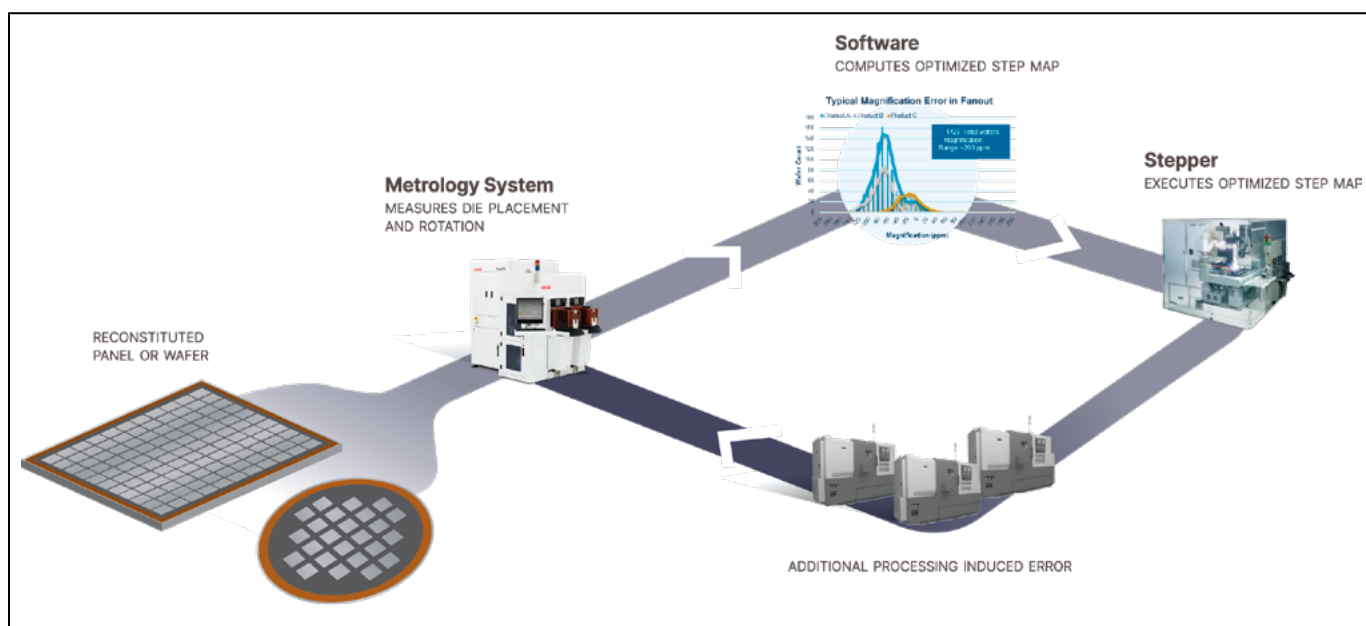


Figure 1: The optimized stepping process loop includes: 1) measurement of die displacement errors outside the stepper; 2) Site correction calculations/yield modeling; and 3) exposure.

placement measurements and pattern overlay registration requirements are continuing to tighten. As a result, the position of the die must be measured before each exposure in the lithography system to ensure accurate registration with the underlying layer. Displacement errors can be measured in the lithography tool, but these measurements are slow, typically taking as much time as the exposure itself. Transferring the measurement operation to a parallel, independent metrology system and feeding corrections to the stepper, however, can double throughput. **Figure 1** illustrates the use of this exposure/measurement loop to increase productivity. The die placement measurements and analysis can be repeated, if required, after each layer is exposed, to correct for any errors introduced in that step. In addition to feed-forward corrections, the software algorithm analyzes the displacement errors to predict yield (based on a user designated limit for acceptable registration error) for exposure fields of varying sizes. The method requires tight integration of the stepper and measurement system with the controlling software algorithm.

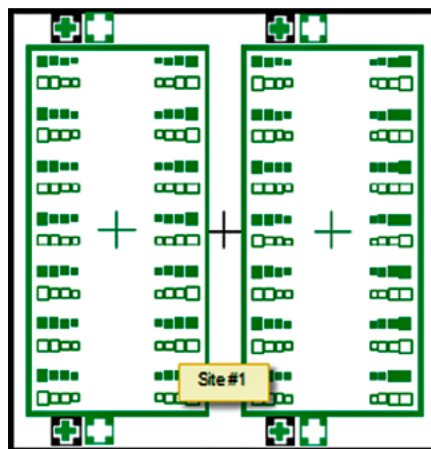


Figure 2: Pad test pattern showing two die.

same method as the wafer study. The test reticle used a single die “Pad” image, which was patterned across the entire panel. The pad test pattern (**Figure 2**), with no offsets, was then measured using the stepper and AOI system at two points per die (top and bottom).

The lithography system (JetStep System, Onto Innovation) supports panel sizes up to 720mm x 600mm.

It uses pattern recognition alignment, allowing the user to train the system to recognize and align on any unique pattern within the field of view. The alignment system can measure the X, Y position of die patterns across the panel, a process often referred to as “mapping.” The AOI system (Firefly System, Onto Innovation) uses a similar pattern recognition alignment method to assess die placement error. Using the stepper and AOI alignment site measurements from the test vehicle panel, a mathematical algorithm was applied to align the stepper and AOI coordinate systems. Once a common grid coordinate system was established, the stepper stage was considered as the reference and the AOI system was compared to this reference using simple scatter plots (**Figure 3**). The measurements were repeated three times to confirm repeatability. In all three cases, accuracy of the AOI system was within $\pm 2.3\mu\text{m}$ of the stepper reference. **Figure 4** shows histograms of the dX and dY distributions for R1. **Table 1** summarizes the statistical data for each run.

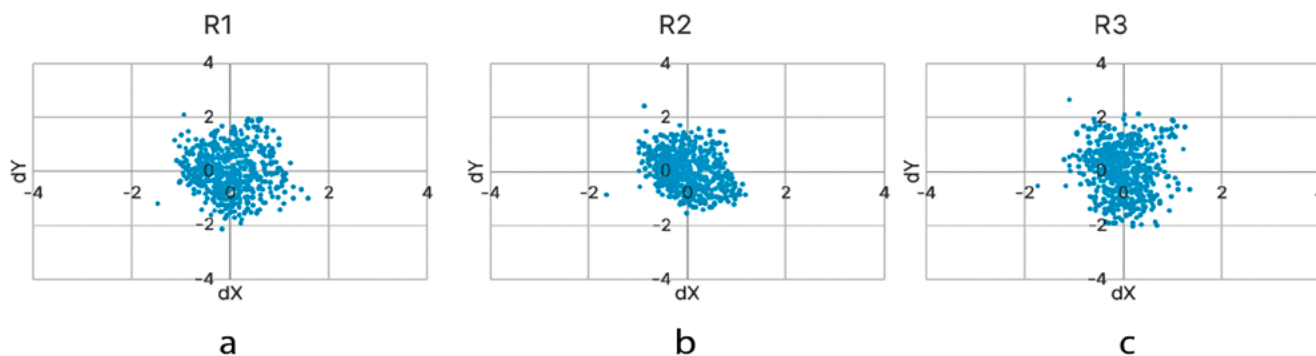


Figure 3: Scatter plots stepper vs. AOI, for three runs: a) R1, b) R2, c) R3.

Coordinate systems; measurement accuracy

A previous study [1] looked at wafer substrates and focused on proving that automated optical inspection (AOI) feed-forward data could correct for the predefined die placement offsets. It established the AOI feed-forward accuracy to be within $\pm 2\mu\text{m}$. The work described below uses a 510mm x 515mm x 1.1mm rectangular glass panel as the test vehicle to match the stepper and AOI panel stage grids and measure the AOI accuracy. The test panel was patterned using the

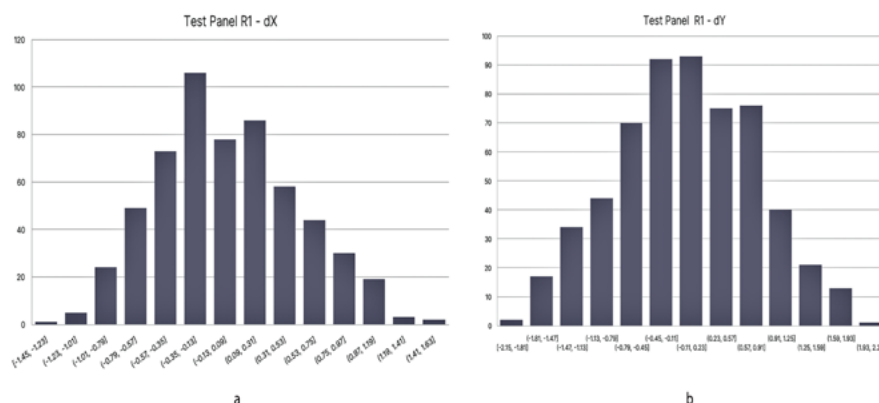


Figure 4: Test vehicle AOI error distributions R1 for a) dX, and b) dY.

| R1 | MEAN | MIN | MAX | RANGE | STD |
|----|---------|---------|--------|--------|--------|
| dx | 3.9E-08 | -1.4487 | 1.5897 | 3.0385 | 0.5174 |
| dy | 8.9E-08 | -2.1498 | 2.0835 | 4.2334 | 0.8043 |

| R2 | MEAN | MIN | MAX | RANGE | STD |
|----|---------|---------|--------|--------|--------|
| dx | 4.5E-06 | -1.6298 | 1.1914 | 2.821 | 0.4670 |
| dy | 4.2E-07 | -1.5700 | 2.4130 | 3.9831 | 0.6828 |

| R3 | MEAN | MIN | MAX | RANGE | STD |
|----|----------|---------|--------|--------|--------|
| dx | -2.3E-07 | -1.7213 | 1.3792 | 3.1005 | 0.4412 |
| dy | -1.9E-08 | -2.0548 | 2.6228 | 4.6776 | 0.9118 |

Table 1: Summary of dX, dY error statistics for R1, R2, R3.

Die placement error measurement

With the accuracy of the measurements and the correspondence between the exposure and measurement coordinate systems established, it is possible to evaluate the placement errors of die on FOPLP panels. Dummy die embedded in molding compound to form a FOPLP substrate were supplied courtesy of ESWIN. Measurements of two points for every die, top and bottom, allowed the system to calculate translation (X,Y) and rotation (Θ) offsets for each. The software algorithm generates

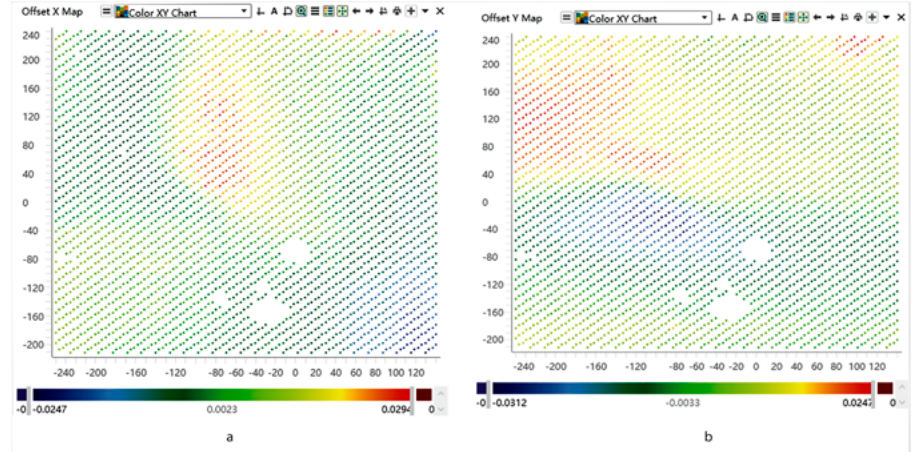


Figure 5: Die placement error (mm) a) dX, and b) dY heat maps.

processing. The disruptive EMC curing effect renders the typical global alignment solution used by lithography tools useless, as it assumes linear corrections for scaling, rotation, orthogonality. Only site-by-site corrections can accommodate these types of errors. To apply site-by-site corrections, each exposure needs to be matched to the local errors to provide good overlay.

Data analysis, yield prediction and throughput

The process specifies overlay errors less than $\pm 15\mu\text{m}$. As long as the measured errors are within the correction capability of the stepper, it is possible to yield 100% by correcting each die, so called “die-by-die” exposure individually, but this imposes an unacceptable penalty on stepper throughput. Increasing the size of the exposure to cover multiple die will

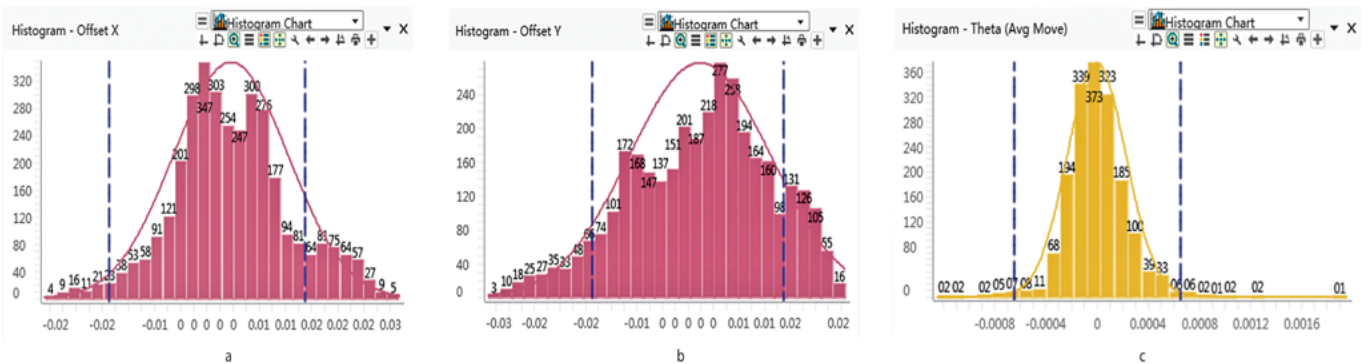


Figure 6: a) dX (mm), b) dY (mm), and c) rotation (rad) data histograms.

“heat maps” that visualize the dummy measurements before corrections are applied (**Figure 5**). Histograms of the X and Y placement errors and rotational errors (**Figure 6**) show the distributions of these measurements.

The multimodal distributions of the dX and dY histograms reflect the nonlinear die placement errors observed in the heat maps. This nonlinear error can be attributed to the epoxy molding compound (EMC) curing process, which is typical for most FOPLP reconstituted panel

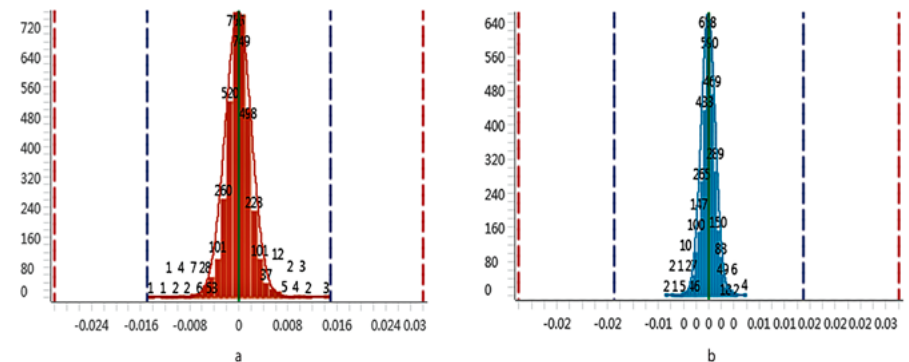


Figure 7: Predicted a) dX and b) dY overlay data histogram (mm) for 3 X 3 field, 100% yield.

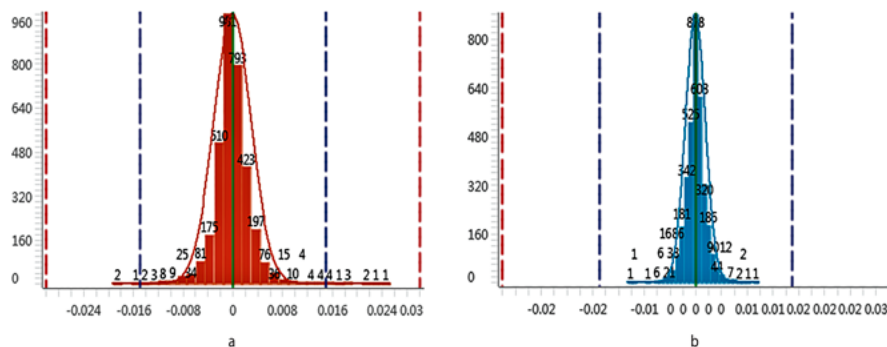


Figure 8: Predicted a) dX and b) dY overlay data histogram (mm) for 6x6 field size, where some die are out of specification, thereby reducing yield.

increase throughput, but reduces the ability to correct for individual die placement errors. By evaluating virtual exposures for different field sizes – and with each exposure corrected to optimize yield within the exposed field – it is possible to maximize process yield (defined as the percentage of die that will meet the overlay specification) and quantitatively evaluate trade-offs between yield and throughput for different field sizes. Only by having real-time data analysis can the user identify the correct settings and react to out-of-control situations without impacting yield.

For the panels evaluated, the software algorithm predicted 100% yield with a field size of 3x3 (**Figure 7**). The dX data was worse than the dY data, but all die placements were within the $\pm 15\mu\text{m}$ via to pad overlay specification. As the stepper field size was increased to 6x6 die, the yield drops to 99.42% as some of the die dX overlay errors exceeded the $\pm 15\mu\text{m}$ specification (**Figure 8**).

The software algorithm's yield prediction has been compared to actual customer product overlay measurements, confirming the accuracy of the prediction is within 0.2% of final overlay results. This result provided the user with confidence that AOI pre-measurement of panels with product die can be used to determine the optimum field size, throughput and yield prior to coating the panel with polyimide or photoresist. This has significant advantages in both cost

and process development. For example, polyimide processing is normally a non-reworkable process step and overlay errors at this stage result in scrapped die. Typically, if there is a die placement error that exceeds the specification of the multi-die exposure field it will only be observed after fully processing the polyimide lithography and measuring overlay. By this time, it would be too late to recover, requiring the die to be scrapped. With the ability to pre-measure and predict the yield with the AOI system and software algorithm, low yield could be avoided by reducing the field size. Moreover, the heat map and histogram data could be sent "upstream" to the EMC process engineer to address the root cause of molding process die placement error excursion.

Summary

It is clear from the experimental data that the calculated feed-forward site corrections provided the stepper with the ability to automatically compensate for die placement error. This is a significant improvement over the industry standard, where steppers use a simple linear model approach. Application of the site corrections, with larger field sizes during stepping, increased the lithography throughput significantly from 3 x 3 to 6 x 6 with low impact on yield, 100% to 99.42% respectively. This will naturally deliver commensurate reductions in cost of ownership.

The visualization of the die placement data using heat maps, histograms, vector plots, etc., provides the process engineer with the ability to optimize and predict the impact of stepper field size on production yield and throughput. Moreover, this revolutionary capability provides foresight, enabling the user to quickly feed data to upstream and downstream processes to prevent costly rework and scrapped product. Future software developments will provide a method to dynamically balance throughput with yield.

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Biography

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